The 9th IEEE International Conference on ASIC

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ASICON 2011

FINAL PROGRAM

Oct. 25-28, 2011

Xiamen International Seaside Hotel,

Xiamen, China

The 9th International Conference on ASIC

ASICON 2011

Oct.25-28, 2011
Xiamen International Seaside Hotel, Xiamen, China

Sponsored by

IEEE Beijing Section
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Contents

Welcome to ASICON 2011

On behalf of the Organizers of the Conference, it is my great pleasure and honor to express our warm welcome to all ASICON 2011 attendees. Thank you very much for your great support to come to Xiamen.

ASICON 2011 is the 9th event of this conference series. The conference will be held from October 25 to 28, 2011 at International Seaside Hotel, Xiamen, China. The conference is intended to provide an international forum for VLSI circuit designers, ASIC users, System Integrators, IC manufacturers and CAD/CAE tool developers to present their updated progresses, developments and research results in their respective fields. The Conference is also intended to afford a platform for attendees to exchange academic and technical information.

This time, the Conference received all together 455 papers from 19 countries and areas. After serious paper review process by more than 100 experts, the TPC of ASICON 2011 has accepted 163 oral papers and 41 invited papers which will be presented in 31 technical sessions.

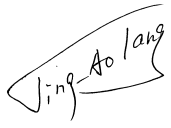
According to the consuetude of international conference, ASICON 2011 invites some famous experts to give five tutorials on the first day of the conference. In addition, we are very pleased to have invited 5 worldwide famous professors and enterprisers to give brilliant Keynote speeches on the plenary sessions from Oct.26-27.

The conference has traditionally a strong impact on both industries and academia. We do hope the peculiar tradition can be strengthened and carried forward through this conference.

This is the third time for ASICON to be held other than Beijing and Shanghai. Xiamen is a very beautiful city. We sincerely hope all of you will have a good time in Xiamen.

General Chair of ASICON 2011

Ting-Ao Tang



2011.10

Conference Committee

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Yongping Xu	National University of Singapore	Singapore
Dunshan Yu	Peking University	China
Danella Zhao	University of Louisiana at Lafayette	USA
Jianjun Zhou	Shanghai Jiao Tong University	China

General Information

● Conference Language

The official language is English. No simultaneous translation is available.

● Conference Schedule

Date	Time	Event
Oct.25 Tue.	AM & PM	Tutorial Session & Registration
Oct.26 Wed.	AM	Opening & Keynote Session
		Keynote Session (K-1,K-2,K-5)
	PM	Parallel Sessions
		Parallel Sessions
		Poster Session (1)
	Evening	Reception
Oct.27 Thu.	AM	Keynote Session (K-3,K-4)
		Parallel Sessions
	PM	Parallel Sessions
		Parallel Sessions
		Poster Session (2)
Oct.28 Fri.	AM	
		Parallel Sessions
	PM	Parallel Sessions
		Parallel Sessions
	Evening	Banquet

● Conference Site

The conference will be held in **Xiamen International Seaside Hotel** (http://www.seaside.cn/english/index1.asp, Tel: 0086-592-5959999, Fax: 592-5959999)**, Xiamen, China,** which locates at **No. 199, Huizhan Er Road, Si Ming District, Xiamen, China.**

● Conference Registration

A. Participant: **Accepted Paper ID Number（if available）:**

☐ Mr. ☐ Ms. First Name: Last Name:

Affiliation (Univ./Company):

Address:

Phone: Fax: Email:

B. Registration Fee

Classification	Before Sep.15, 2011	After Sep.15, 2011	Amount
IEEE or IET member★	☐ RMB 3400（or USD 540）	☐ RMB 3700 (or USD 588	
Non-member	☐ RMB 3700 (or USD 588)	☐ RMB 4000 (or USD 635)	
Student	☐ RMB2100 (or USD 335)	☐ RMB 2400 (or USD 380)	
Extra banquet ticket	☐ RMB 300 (or USD 50)		
Extra pages	☐ RMB 400 / page （or USD 60/page）		
Tutorials	☐ T-1+T-2+T-3+T-4 RMB 200 (USD 30) ☐ T-5 RMB 150 (or USD 25)		
☐ Vegetarian	☐ Need hardcopy Proceedings RMB 500 (or USD 80) ☐ Don't need hardcopy Proceedings		
Total Amount	RMB Or USD		

(★IEEE or IET Member) ★ Member Number: _____

The registration fee covers:

- Admission to all the sessions;
- Three days' meals (Oct. 26 - Oct. 28, 2011) including the reception (Evening of Oct. 26) and the banquet (Evening of Oct. 28); Coffee Breaks;
- A conference kit (with a conference bag, a program brochure, and a USB-disk).

(The tutorial fee covers the lunch (Oct. 25) and tutorial materials. Please visit the conference website for details of the tutorials.)

● Registration Desk

The conference registration desk will be located at Xiamen International Seaside Hotel. The

conference registration will be open on Oct. 25 (8:00-20:00), Oct. 26 (8:00-17:45), Oct.27 (8:00-17:45). And the registration desk will keep available at the same site throughout the whole conference.

● Transportation

Located in the southeast of China, Xiamen is a coast city of Fujian Province. With convenient transportation, there are more than 10 flights from main cities such as Beijing, Shanghai and Guangzhou to Xiamen everyday.

Being accessible to the hotel, it is only 15 minutes' ride by taxi from Xiamen Gaoqi International Airport, 20 minutes' from the railway station, and 25 minute's from the ferry.

● Weather

The average temperature during conference time in Xiamen is around 18℃~28℃.

● Visa

All the foreign travelers to China must have a valid visa. Visas may be obtained from the Chinese Embassy or Consulate in most major cities around the world. A conference attendee will be mailed an official invitation letter for visa application after he or she fills and returns the Visa Application Form (http://www.asicon.org) to asicon_org@fudan.edu.cn timely.

● Awards

Excellent Student Paper Awards will be announced at the banquet on Oct.28. To be qualified for the Excellent Student Paper Award, the paper must be presented by the student himself or herself (1st author). The Technical Program Committee and Organizing Committee will choose through public appraisal some excellent student papers from the candidates.

Paper Presentation Information

The ASICON-2011 will have oral and poster sessions. All the papers included in the conference program should be presented in English by one of the authors at the arranged sessions.

● Oral Presentation

Presentation time:

Invited paper (30 minutes): 25 min talk + 5 min Q/A

Regular paper (15 minutes): 12 min talk + 3 min Q/A

Computer and digital projector will be provided in each meeting room.

● Poster Presentation

Poster size: 120 cm (high) × 100 cm (wide)

Poster Session 1:

Setup time: 8:30-17:30 on Oct. 26

Presentation time: 17:45-18:45 on Oct.26 (on the spot)

Display time: 8:30-21:00 on Oct.26

Poster Session 2:

Setup time: 8:30-17:30 on Oct. 27

Presentation time: 17:45-18:45 on Oct.27 (on the spot)

Display time: 8:30-21:00 on Oct.27

Thumb pins, adhesive tapes, and scissors will be provided at the registration desk. The poster should be taken off by 21:30 by the author if he or she would like to keep it. After that time, it will be removed and be regarded as being discarded by the authors.

● Coffee Break

Complementary coffee/tea will be served in each morning/afternoon session. The break will take place in general at 10:00-10:15 during morning sessions and 15:30-15:45 during afternoon sessions. Due to time schedule of different sessions, the actual break time may have slight variation. Coffee/tea will be served in about half-hour duration.

● Meeting Room Location

Meeting Room	Actual Room Name
Room 6	Sea-View Meeting Room 6
Room 7	Sea-View Meeting Room 7
Room 8	Sea-View Meeting Room 8
Room 9	Sea-View Meeting Room 9
Poster	Koron Banquet Hall

Tutorial Session

Tuesday, October 25, 9:00 – 12:00

Tuesday, October 25, 9:00 – 12:15 Room 6
Tutorial Session (I)

T-1 **Spintronic Devices – the Future Storage and Computing Elements in Computing Systems**
Hai (Helen) Li (Polytechnic Institute of New York University, USA)

T-2 **What You Need to Know for Effective CDC Verification**
Jin Zhang (Real Intent, USA)

Tuesday, October 25, 9:00 – 11:00 Room 7
Tutorial Session (II)

T-5 **CMOS device and silicon scaling for SoC**
Peng Bai (Intel, USA)

Tuesday, October 25, 14:00 – 17:00

Tuesday, October 25, 14:00 – 17:00 Room 6
Tutorial Session (III)

T-3 **A New Approach for Power Aware Design and Verification Using Sequential Analysis Technology**
Anmol Mathur (Calypto Design Systems)

T-4 **Chip-Package-System Co-Design for High Speed Switching Fabric ASIC**
Shaofeng (Tony) Luan, Bonnie Lee, Shahriar Mokhtarzad, Linming Jin
(Brocade Communications Systems Inc., , USA)

Technical Session

Wednesday

Wednesday, October 26, 8:30 – 12:15

Wednesday, October 26, 9:00 – 12:15 International Auditorium

Keynote Session (I)

K-1 **Transistors and Conpact Models for 20 nm node and beyond**

Chenming Hu (UC Berkeley, USA)

K-2 **Components of the successful SOC ASIC design**

Tom Bedna (IBM, USA)

K-5 **The New Development of EDA Tools for VLSI Design**

Paul Lo (Synopsys, USA)

Wednesday, October 26, 13:30 – 15:30

Wednesday, October 26, 13:30 – 15:30 Room 6
Session 4J: Reference & Nyquist Analog-to-Digital Converters (Ⅱ)

	Title
4J-1	**Energy efficient ADC design with low voltage operation(invited paper)**
13:30	Akira Matsuzawa(Tokyo Institute of Technology,Japan)
4J-2	**A low-power 4.224GS/s Sampler in 0.13-μm CMOS for IR UWB Receiver**
14:00	Yi Zhao, Jun Jiang, Ke Shao, Yajie Qin, Zhiliang Hong(Fudan University, China)
4J-3	**CMOS low-power subthreshold reference voltage utilizing self-biased body effect**
14:15	Zhang Hao , Zhang Yimeng , Huang Mengshu, Yoshihara Tsutomu(Waseda University, Japan)
4J-4	**A Precision 2.5V Bandgap Voltage Reference with Excellent Initial Accuracy of 0.25% for High Resolution ADCs**
14:30	Xiaozong Huang, Jing Zhang, Luncai Liu, Wengang Huang, Yanlin Zhang ,Lei Yu(Sichuan Institute of Solid-state Circuits, China)
4J-5	**A High-Performance Bandgap Reference with Advanced Curvature-Compensation**
14:45	Zekun Zhou, Xiangzhu Xu, Yue Shi, Xin Ming, Bo Zhang(University of Electronics Science and Technology of China, China)

Wednesday, October 26, 13:30 – 15:30 Room 8
Session 1A: VLSI Design and Circuits (Ⅰ)

	Title
1 A-1	**High Speed Area Reduced 64-bit Static Hybrid Carry-Lookahead/Carry-Select Adder**
13:30	Habib Ghasemizadeh Tamar(Urmia Microelectronic Research Laboratory, Iran),Akbar Ghasemizadeh Tamar, Khayrollah Hadidi, Abdollah Khoei&AghilAhmadi (*K.N. Toosi Univ. of Technology, Iran*)
1A-2	**A Behavior-based Reconfigurable Cache for the Low-power Embedded Processor**

13:45	Jiongyao Ye, Jiannan Jin , Tabkahiro Watanabe (*Waseda University, Japan*)
1A-3	**A Novel Method for Storage Architecture of Pipeline FFT Processor**
14:00	Ting Zhang, Lan Chen, Yan Feng (*Chinese Academy of Sciences, China*)
1A-4	**Design of Resistant DPA Three-valued Counter Based on SABL**
14:15	Yuejun Zhang (*Ningbo University, China*), Pengjun Wang(*Fudan University, China*), Lipeng Hao(*Ningbo University, China*)
1A-5	**Improvement of Adiabatic Domino Circuits and its Application in Multi-valued Circuits**
14:30	Qiankun Yang ,Pengjun Wang, Fengna Mei (*Ningbo University, China*),
1A-6	**Low Power Shift Registers for Megabits CMOS Image Sensors**
14:45	Jinn-Shyan Wang, Tsung-Han Hsieh, Keng-Jui Chang, and Chingwei Yeh (*Chung-Cheng University, Taiwan*)
1A-7	**High-parallel LDPC decoder with power gating design**
15:00	Ying Cui1, Xiao Peng, Yu Jin, Peilin Liu, Shinji Kimura, Satoshi Goto (*Waseda University*)
1A-8	**A Reconfigurable Macro-Pipelined DCT/IDCT Accelerator**
15:15	Wenqi Bao, Jiang Jiang, Qing Sun, Yuzhuo Fu (*Shanghai Jiao Tong University, China*)

Wednesday, October 26, 13:30 – 15:30 Room 7
Session 1F: Advanced Memory (Ⅰ)

	Title
1F-1	**Current Status and Future Prospect of Phase Change Memory(invited paper)**
13:30	Byeungchul Kim(Semiconductor R&D Center, Samsung Electronics Co., Korea), Yoonjong Song, Sujin Ahn, Younseon Kang, Hoon Jeong, Dongho Ahn, Seokwoo Nam, Gitae Jeong, Chilhee Chung
1F-2	**Memristor Models and Circuits for Controlling Process-VDD-Temperature Variations(invited paper)**
14:00	Kwan-Hee Jo, Chul-Moon Jung, and Kyeong-Sik Min(School of Electrical Engineering, Kookmin University, Korea)
1F-3	**The Design of Low Leakage SRAM Cell with High SNM**
14:30	Hao YAN(Digital System Integration Lab, Institute of Acoustics, Chinese Academy

	of Sciences,and Graduate University of Chinese Academy of Sciences Beijing, China),*, Donghui WANG, Chaohuan HOU(Digital System Integration Lab, Institute of Acoustics, Chinese Academy of Sciences)
1F-4	**Novel RRAM Programming Technology for Instant-on and High-security FPGAs**
14:45	Xiaoyong Xue, Wenxiang Jian, Yufeng Xie, Qing Dong, Rui Yuan, Yinyin Lin(Fudan University, China)
1F-5	**A Study of Dual-Vt Configurations of an 8T SRAM Cell in 45nm**
15:00	Wenbin Liu, Jinhui Wang,Wuchen Wu, Xiaohong Peng, Ligang Hou(Beijing University of Technology, Beijing China)

Wednesday, October 26, 13:30 – 15:30 Room 9
Session 2R: Wireless transceiver and building blocks (Ⅱ)

	Title
2R-1	**A Low Noise and Highly Linear 2.4-GHz RF Front-End Circuit for Wireless Sensor Networks(invited paper)**
13:30	Chihoon Choi, Joonwoo Choi, and Ilku Nam(Pusan National University, Korea)
2R-2	**An Auto-calibrating I/Q Mismatch Scheme for High Image Rejection GPS RF Receiver**
14:00	Lijiong Wang, Tingting Mo, Dongpo Chen(*Shanghai Jiao Tong University, China*)
2R-3	**A Dual-mode Analog Baseband Utilizing Digital-assisted Calibration for WCDMA/GSM Receivers**
14:15	Renzhong Xie, Chen Jiang, Weinan Li, Yumei Huang ,Zhiliang Hong(*Fudan University, China*)
2R-4	**A 0.25dB Gain Step High Linear Programmable Gain Amplifier**
14:30	Xiaobin Shen, Taotao Yan, Yuxiao Lu, Jianjun Zhou(*Shanghai Jiao Tong University, China*)
2R-5	**Reconfigurable Low Pass Filter with Automatic Frequency Tuning for WCDMA and GSM Application**
14:45	Chen Jiang, Renzhong Xie,Weinan Li, Yumei Huang and Zhiliang Hong(*FudanUniversity, China*)

2R-6	**A Wide Tuning Range Low-pass Gm-C Filter for Multi-Mode Wireless Receivers with Automatic Frequency Calibration**
15:00	Yu Wang, Na Yan, Hao Min(*Fudan University , China*)
2R-7	**RFIDsense: a Reconfigurable RFID Sensor Tag Platform Conforming to IEEE 1451.7 Standard**
15:15	Feibai Zhu, Min Li, Haichao Han, Junyu Wang(*Fudan University, China*)

Wednesday, October 26, 15:45-17:45

Wednesday, October 26, 15:45-17:45 Room 6
Special Session: ESL Design

	Title
1S-1	**Architecture and Design Automation for Application-Specific Processors(invited paper)**
15:45	Philip Brisk(University of California, Riverside, USA)
1S-2	**High-Level Synthesis: On the Path to ESL Design(invited paper)**
16:15	Philippe COUSSY, Dominique HELLER, Cyrille CHAVET(Université de Bretagne-Sud, France)
1S-3	**Study of High-Level Synthesis: Promises and Challenges(invited paper)**
16:45	Kyle Rupnow, Yun Liang, Yinan Li(Advanced Digital Sciences Center), Deming Chen(University of Illinois at Urbana-Champaign)
1S-4	**On Virtual Prototying of Embedded System-on-Chip(invited paper)**
17:15	Yi Ni, Wai Sum Mong, Jianwen Zhu(University of Toronto, Canada)

Wednesday, October 26, 15:45-17:45 Room 9
Session 1O: Clock Synthesizer and Building Blocks (Ⅰ)

	Title
1O-1	**A Study of Frequency Synthesizer for AT-DMB Applications(invited paper)**
15:45	Jun Cheng, Yong Moon(*Soongsil University, South Korea*)

1O-3	**A New Figure of Merit of LC Oscillators Considering Frequency Tuning Range**
16:30	Takahiro Sato, Kenichi Okada and Akira Matsuzawa(*Tokyo Institute of Technology, Japan*)
1O-4	**Low Noise Low Power Two-Stage Modulator With Injection Locked LO Divider in 65nm CMOS**
16:45	Wufeng Wang, Peichen Jiang, Tingting Mo, Jianjun Zhou(*Shanghai Jiao Tong University, China*)
1O-5	**Design of a Low-Power Low-Phase-Noise Multi-Mode Divider With 25%-Duty-Cycle Output in 0.13um CMOS**
17:00	Song Hu, Weinan Li, Yumei Huang, Zhiliang Hong(*Fudan University, China*)

Wednesday, October 26, 15:45 – 17:45 Room 8 Session 2A: VLSI Design and Circuits (Ⅱ)

	Title
2 A-1	**Scheduling to Timing Optimization for a Novel High-level Synthesis Approach**
15:45	Ling Li, Teng Wang, Ziyi Hu Xin'an Wang, Xu Zhang(*Peking University Shenzhen Graduate School, China*)
2A-2	**High Reliable Digital Signal Processor for Automotive Application**
16:00	Yimiao Zhao, Zhigang Ni (*Beijing Design Center, Analog Devices, China*)
2A-3	**A Novel Differential Fault Analysis on AES-128**
16:15	Pengjun Wang(*Fundan University, Shanghai 201203, China, Ningbo University, China*), Lipeng Hao (*Ningbo University, China*)
2A-4	**Saving 78.11% Dhrystone power consumption in FPU by clock gating while still keeping co-operation with CPU**
16:30	Minh Thien Trieu, Huong Thien Hoang, Phong The Vo, Hung Bao Vo(*Renesas Design Vietnam Company Ltd., Vietnam, Renesas Electronic Corporation Tokyo, Japan*),Yoichi Yuyama(*Renesas Electronic Corporation Tokyo, Japan*)
2A-5	**A hardware/software co-design approach for multiple-standard video bitstream parsing**

16:45	Sha Shen, Huibo Zhong, Yibo Fan, Xiaoyang Zeng(*Fudan University, China*)
2A-6	**ADDLL/VDD-Biasing Co-design for Process Characterization, Performance Calibration, and Clock Synchronization in Variation-Tolerant Designs**
17:00	Jinn-Shyan Wang, Yung-Chen Chien, Jia-Hong Lin, Chun-Yuan Cheng, Ying-Ting Ma, Chung-Hsun Huang(*Chung-Cheng University, Taiwan*)
2A-7	**Analysis of Adaptive Support-Weight Based Stereo Matching for Hardware Realization**
17:15	Junbao Liu, Shuai Wang, Yang Li, Jun Han,Xiaoyang Zeng(*FudanUniversity, China*)
2A-8	**A High Performance Sound Source Localization System based on Macro-pipelined Architecture**
17:30	Qing Sun, Yuzhuo Fu, Wenqi Bao, Jiang Jiang(*Shanghai Jiao Tong University, China*)

Wednesday, October 26, 15:45-17:45 Room 7 Session 2E: Testing, Reliability, Fault-Tolerance (Ⅱ)

	Title
2E-1	**Challenges of Electrostatic Discharge (ESD) Protection in Emerging Silicon Nanowire Technology(invited paper)**
15:45	Juin J. Liou(Pegasus Distinguished Professor, University of Central Florida, Orlando, Florida, USA),Chang Jiang (Scholar Endowed Professor, Ministry of Education, China),Cao Guang-Biao(Endowed Professor, Zhejiang University, China) Chang Gung (Endowed Professor, Chang Gung University, Taiwan) Feng Chia(Endowed Professor, Feng Chia University, Taiwan)
2E-2	**A Software/Hardware Co-Debug Platform for Multi-Core Systems(invited paper)**
16:15	Kuen-Jong Lee, Long-Feng Chen, Jia-Wei Jhou(Department of Electrical Engineering, National Cheng Kung University, Tainan, Taiwan), Alan Su ,Jiff Kuo, Mark Liu(Global UniChip Corporation, HsinChu, Taiwan)
2E-3	**HV CMOS Orientated Variation-aware Layout and Robust Solution**
16:45	Gu Cong, Chen Hong(Design Enable Group, RASG, Freescale Semiconductor Ltd , Beijing, China)
2E-4	**Modified Minimal-Connected-Component Fault Block Model to Deal with**

	Defective Links and Nodes for 2D-Mesh NoCs
17:00	Yueming Yang, Heng Quan, Zewen Shi, Xiaoyang Zeng, Zhiyi Yu(State Key Laboratory of ASIC & System, Fudan University, Shanghai, China)
2E-5	**Addressing Fault Tolerance in 4-PAM Signaling by Using Block Codes for On-chip Communication**
17:15	Arash Abtahi Forooshani, Fakhrul Zaman Rokhani(Department of CCSE, University Putra Malaysia, Serdang Malaysia)
2E-6	**A Novel Multi-finger Layout Strategy for GGnMOS ESD Protection Device**
17:30	Peng Zhang, Yuan Wang, Song Jia, Xing Zhang(Key Laboratory of Microelectronic Devices and Circuits, Peking University, China)

Wednesday, October 26, 17:45 – 18:45

Wednesday, October 26, 17:45 – 18:45 Hall

Post Session (I)

	Title
PA01	**A Thermal Model for the Top Layer of 3D Integrated Circuits Considering Through Silicon Vias**
	Fengjuan Wang, Zhangming Zhu, Yintang Yang, Ning Wang (Xidian University , China)
PA02	**Novel High Uniformity Readout Circuit Allowing Microbolometer to Operate with Low Noise**
	Jian Lv*, Yun Zhou, Baobin Liao, Yadong Jiang(University of Electronic Science and Technology of China, China)
PA03	**Monolithic Broadband power Amplifier using AlGaN-GaN on Sic**
	Huizhi Wang, Liang Li(Science and Technology on ASIC Lab, China), Yuxing Cui(Heibei Semiconductor Research Institute, China),Jiayun Yin(Science and Technology on ASIC Lab, China),Zhihong Feng(Science and Technology on ASIC Lab, China),Hongjiang Wu(Heibei Semiconductor Research Institute, China)
PA04	**Integration of information security chips based on System-in-Package**
	Tong Ran , Guoqiang Bai(Tsinghua University, China)
PA05	**A New Asynchronous Delay-Insensitive Link based on a 1-of-4 LETS Code**
	Can Wang, Qin Wang, Jianfei Jiang (Shanghai Jiao Tong University, China)
PA06	**A High-speed Asynchronous Array Multiplier based on Multi-threshold Semi-Static NULL Convention Logic Pipeline**
	Yanfei Yang,Yintang Yang, Zhangming Zhu, Duan Zhou (XiDian University, China)
PA07	**An Ultra Low Power ASK Demodulator for Passive UHF RFID Tag**
	Hongqiang Zong, Jinpeng Shen, Shan Liu, Mei Jiang, Qingyuan Ban, Ling Tang, Fanyu Meng, and Xin'an Wang(Peking University Shenzhen Graduate School, China)
PA08	**Improvement and Parallel Implementation of Canny Edge Detection Algorithm Based on GPU**
	Shengxiao Niu, Jingjing Yang, Sheng Wang, Gengsheng Chen(Fudan University, China)
PA09	**A New Full Current Mode Sense Amplifier with Compensation Circuit**

	Yiqi Wang, Fazhao Zhao, Mengxin Liu, Zhengsheng Han (Chinese Academy of Sciences, China)
PA10	**An Efficient 90nm Technology-Node GHz Transceiver of On-Chip Global Interconnect**
	Zaixiao Zheng, Zhigang Mao, Jianfei Jiang (Shanghai JiaoTong University, China)
PA11	**Electrochemical Biosensor Based on Modified Graphene Oxide for Tuberculosis Diagnosis**
	Pei Zhang, Xiaosen Chai, Chun Xu, Jia Zhou(Fudan University, China)
PA12	**Digital Quadrature IF modulator using single-bit DACs**
	RuiminHuang,ChaodongLing,JiaxianWang(HuaqiaoUniversity, China)
PA13	**Zero-Crossing Distortion Analysis in One Cycle Controlled Boost PFC for Low THD**
	Yani LI, Yintang YANG , Zhangming ZHU (Xidian University, China), Wei Qiang (Xi'an Longtium Microelectronics Technology Developing Co., Ltd, China)
PA14	**A Simulation Study of Vertical Tunnel Field Effect Transistors**
	Zhong-Fang Han, Guo-Ping Ru*, Gang Ruan(Fudan University, China)
PA15	**Determination of the trap states distribution in Poly-Si films using the OEMS modulation**
	Xiyue Li, Wanling Deng, Junkai Huang(Jinan University, China)
PA16	**High efficiency and low power multi-rate LDPC decoder design for CMMB**
	Jiang xiaobo, li hongyuan (South China University of Technology, Chain)
PA17	**Area efficient LDPC decoder design for parallel layered decoding**
	Yuan Yao, Fan Ye, and Junyan Ren(Fudan University, China)
PA18	**(paper withdraw)**
PA19	**Accelerating the Data Shuffle Operations for FFT Algorithms on SIMD DSPs**
	Kai Zhang1*, Shuming Chen1, Sheng Liu1, Yaohua Wang1, Junhui Huang1 (1 School of Computer, National University of Defense Technology, Changsha 410073, China)
PA20	**Automatic Compilation Flow for a Coarse-grained Reconfigurable Processor**
	Hao Wang, Weiguang Sheng, Weifeng He (Shanghai Jiao Tong University, China)
PA21	**Origin of High On-State Current For Dopant-Segregated Schottky MOSFET**
	Yang Tang, Liu-Lin Zhong, and Yu-Long Jiang (Fudan University, China)

PA22	**System Level Performance Evaluation of Three-Dimensional Integrated Circuit**
	Libo Qian*, Zhangming Zhu, Yintang Yang(Xidian University, China)
PA23	**An Energy Efficiency Task Scheduling Algorithm for Streaming Applications on Multiprocessor SoC**
	Shan Cao*, Zhaolin Li, and Shaojun Wei(Tsinghua University, China)
PA24	**Analysis and Architecture Design of Aggregation in BM3D**
	Wenjiang Liu1*, Yue Zhu, Tao Liu, Mengtian Rong, Hao Zhang (Shanghai Jiao Tong University, China)
PA25	**A JTAG-based Configuration Circuit applied in SerDes Chip**
	Xun Jiang, Xiaoxin Cui*, Dunshan Yu(Peking University, China)
PA26	**An Automated Design Flow for Image Processing Filter in Embedded Systems**
	Akitoshi Matsuda(Kyushu University, Japan), Shinichi Baba(Kyushu Embedded Forum, Japan)
PA27	**A Novel Channel Estimation Algorithm in OFDM Power Line Communication System**
	Huidong Zhao*, Yong Hei, Shushan Qiao(Institute of Microelectronics of Chinese Academy of Sciences, China) *Email:hdzhao2003@126.com
PA28	**Low Power Design for SoC with Power Management Unit**
	Daying Sun, Shen Xu, Weifeng Sun, Shengli Lu, Longxing Shi (Southeast University, China)
PA29	**Improvement on Branch Scheduling for VLIW Architecture**
	Lidan Bao, Hongmei Wang, Tiejun Zhang, Donghui Wang, Chaohuan Hou (Chinese Academy of Sciences, China)
PA30	**Research on Reconfigurable Multiplier Unit Based on GF[(28)]4 Field of Symmetric Cryptography**
	Xu JianBo, Dai Zibin(Zhengzhou Information Science and Technology Institute, China), Xuan Yang (Jiangnan Institute of Computing Technology ,China) Su Yang(Zhengzhou Information Science and Technology Institute, China)
PA31	**A Low-Voltage Differential Injection Locked Divider with Forward Body Bias**
	Haipeng Fu, Hanchao Zhou, Yangyang Niu, Junyan Ren*, Wei Li*, Ning Li(Fudan University, Shanghai, China)
PA32	**Effects of unintended dopants on I-V characteristics of the double-gate**

	MOSFETs, a simulation study
	Peicheng Li, Guanghui Mei, Guangxi Hu*, Ran Liu, and Tingao Tang(Fudan University, China)
PA33	**A Control Scheme for a 65nm 32×32b 4-read 2-write Register File**
	Jun Han, Xingxing Zhang, Baoyu Xiong, Zhiyi Yu*, Xiaoyang Zeng (Fudan University, China)
PA34	**Reflection Analysis of Signal Transmission in 32-bit CPU Based SiP**
	Zerong Tao, Liji Wu*, Xiangmin Zhang (Tsinghua University, China)
PA35	**Research on Testing of 32-bit CPU Based SiP**
	Chunlin Xie, Liji Wu*, Xiangmin Zhang (Tsinghua University, China)
PA36	**A Confidential RFID Model to Prevent Unauthorized Access**
	*Maryam Gharooni, Mazdak Zamani (Universiti Teknologi Malaysia), Mehdi Mansourizadeh(Multimedia University), Shahidan Abdullah(Universiti Teknologi Malaysia)
PA37	**A Security Processor Based on MIPS 4KE Architecture**
	Shuai Wang1, Yang Li, Junbao Liu, Jun Han*, and Xiaoyang Zeng(Fudan University, China)
PA38	**Design of A Reconfigurable Network Interface Processor**
	Lei Zhang (Xi'An University of Posts and Telecom, China), Tao Li(Shaanxi Provincial Research Center of Telecom ASIC Design, China), Zhentao Li , Lin Jiang(Xi'An University of Posts and Telecom, China)
PA39	**A Hardware Accelerator for Speech Recognition Applications**
	Tao Chen,Jiawei Zheng, Xingsi Zhang, Shengchang Cai, YunChen(Fudan University, China)
PA40	**A Programmable IP Core for LDPC Decoder Based on ASIP**
	Jun Deng(Sichuan Institute of Solid-state Circuits, China), Bing Li(Southeast University, China), Lintao Liu(Science and Technology on Analog Integrated Circuit Laboratory, China),Rui Chen(Southeast University, Nanjing, 210096, China)
PA41	**Parallel Structure of GF (2^14) and GF (2^16) Multipliers Based on Composite Finite Fields**
	Jianing Su, Zhenghao Lu*(Soochow University, Suzhou, China)
PA42	**Novel CMOS Schmitt triggers using floating-gate MOS transistors**
	Guoqiang Hang (Zhejiang University City College, China)(Zhejiang University, China) , Hongli Zhu(Zhejiang University City College, China), Peiyi Zhao(Chapman

	University, USA), Xuanchang Zhou(Zhejiang University City College, China)
PA43	**A New Method to Improve the Unconditional Stability of InGaP/GaAs Heterojunction Bipolar Transistor**
	Shanggong Feng1, Yanhu Chen, Huijun Li(Shan Dong University, China), Minghua Zhang(Artillery Command Academy, China)
PA44	**An Accurate Physics-Based Method for Calculating DC Inductance of On-chip Square Multi-layer Inductors**
	Jinran Du, Wanghui Zou, Xuecheng Zou(Huazhong University of Science and Technology, China)
PA45	**Dual Frequency Based Real Time Location System Using Passive UHF RFID**
	Junjuan Liu, Xi Tan, Hao Min (Fudan University, China)
PA46	**NoC buffer allocation strategy based on flow distribution table**
	Zhouyi Liu, Chiu-Sing Choy(The Chinese University of Hong Kong, Hong Kong)
PA47	**A Reconfigurable Linear Array Processor Architecture for Data Parallel and Computation Intensive Applications**
	Yucheng Liu, Jing Xie, Zhigang Mao (Shanghai Jiao Tong University, China)
PA48	**A permutation network for configurable and scalable FFT processors**
	Shuai Chen, Jialin Chen, Kanwen Wang, Wei Cao*, Lingli Wang, Member, IEEE(Fudan University, China)
PA49	**Comparison of 2D MESH Routing Algorithm in NOC**
	Pan Hao,Hong Qi, Du Jiaqin,Pan Pan(Anhui University, China)
PA50	**Simulation of Carrier Transport in Quantum Cascade Lasers**
	Yingying Li, Guo-Ping Ru(Fudan University, China), Z.-M. Simon Li(Crosslight Software Inc., Canada)
PA51	**Design of a UHF RFID Tag Baseband with the Hummingbird Cryptographic Engine**
	Mengqin Xiao, Xiang Shen and Junyu Wang(Fudan University, China), Joseph Crop (Oregon State University, USA)
PA52	**A study on channel polarization and polar coding**
	Yichao Lu, Satoshi Goto (WASEDA UNIVERSITY, Japan)
PA53	**A Novel Linear Power Amplifier for 2.6GHz LTE applications**
	Jianbao Deng*, Shilin Zhang, Luhong Mao, Sheng Xie, Huichao Li(*Tianjin University, China*)

PA54	**Design of a Monolithic Low-power Micro-sensor Signal Processing System**
	Zhuping Wang, Keshu Zhang(Chinese Academy of Sciences, China)

Thursday

Thursday, October 27, 8:30 – 10:00

Thursday, October 27, 8:30 – 10:00 International Auditorium

Keynote Session (II)

K-3 **Who Needs Electrons?**

Edoardo Charbon (TU Delft，The Netherlands)

K-4 **Low Power LSI Design Methods Based on Gating Technology”**

Shinji Kimura (Waseda Univerisity, Japan)

Thursday, October 27, 10:15 – 12:15

Thursday, October 27, 10:15 – 12:15 Room 8
Session 3A: VLSI Design and Circuits (III)

	Title
3 A-1	**Research on Design of A Reconfigurable Parallel Structure Targeted at LFSR**
10:15	Wei Li(*the Information Engineering University, China*), Xuan Yang(*Jiangnan Institute of Computing Technology, China*), Zibin Dai(*the Information Engineering University, China*)
3A-2	**Using NOC technology to improve Photoelectric Encoder system for LAMOST spectroscopes**
10:30	Zhongyi Han(*Chinese Academy of Sciences, China, Chinese Academy of Sciences, China, Graduate University of Chinese Academy of Sciences, China*), Jianing Wang(*Chinese Academy of Sciences, China, Chinese Academy of Sciences, China)*, Yizhong Zeng(*Chinese Academy of Sciences, China, Chinese Academy of Sciences, China)*, Zhongwen Hu(*Chinese Academy of Sciences, China, Chinese Academy of Sciences, China)*
3A-3	**A New Configurable Logic Block with 4/5-input Configurable LUT and Fast/Slow-Path Carry Chain**
10:45	Zhidong Mao, Liguang Chen, Yuan Wang, Jinmei Lai(*Fudan University, China*)
3A-4	**A 768 Megapixels/sec Inverse Transform With Hybrid Architecture For Multi-Standard Decoder**
11:00	Tuan Minh Phan Ho, Thang Minh Le, Khanh Duy Vu(*Renesas Design Vietnam Company, Ltd, Vietnam*) Seiji Mochizuki, Kenichi Iwata, Keisuke Matsumoto, Hiroshi Ueda(*Renesas Electronics Corporation, Japan*)
3A-5	**A Two-way Parallel CAVLC Encoder for 4Kx2K H.264/AVC**
11:15	Huibo Zhong, Sha Shen, Yibo Fan, Xiaoyang Zeng(*Fudan University, China*)
3A-6	**Multi-Stage Power Gating Based on Controlling Values of Logic Gates**
11:30	Yu JIN(*Waseda University, Japan*), Shinji KIMURA
3A-7	**A High Speed Reconfigurable Face Detection Architecture**
11:45	Weina Zhou(*Fudan University, China, Shanghai Maritime University, China*), Yao Zou, Lin Dai, Xiaoyang Zeng((*Fudan University, China*)
3A-8	**A Coarse-grained Reconfigurable Computing Unit**
12:00	Kanwen Wang, Shuai Chen, Wei Cao, Lingli Wang(*Fudan University, China*)

Thursday, October 27, 10:15 – 12:15 Room 6
Session 1J: Analog Filters and Oversampling Data Converters

	Title
1J-1	**Cascadable Current-Mode Multifunction Filter Configuration Using Minimum Number of CCTAs and Grounded Capacitors**
10:15	Xifeng Zhou,Jinguang Jiang , Shanshan Li(Wuhan University,China)
1J-2	**A matrix approach to low-voltage low-power log-domain CMOS current-mode adjustable-bandwidth step-gain filter design**
10:30	Xiaoyu Wang, Haigang Yang, Tao Yin, Fei Liu(Chinese Academy of Sciences, China)
1J-3	**A Sigma-Delta Modulator with a Novel Chopper Correlated Double Sampled Integrator**
10:45	Luo Wang, Huihui Ji(Beihang University, China), Quan Sun(Chinese Academy of Sciences, China)
1J-4	**VLSI Implementation of High-Speed Low Power Decimation Filter for LTE Sigma-Delta A/D Converter Application**
11:00	Jing Li, Ran Li, Ting Yi, Zhiliang Hong(Fudan University, China), Bill Yang Liu(Analog Devices, China)
1J-5	**A Continuous Time Sigma-Delta Modulator Using Time-Domain Quantizer and Feedback Element**
11:15	Siliang Hua, Hao Yan, Yan Liu, Donghui Wang, Chaohuan Hou(Chinese Academy of Sciences, China)
1J-6	**An Analysis on a Pseudo-Differential Dynamic Comparator with Load Capacitance Calibration**
11:30	Daehwa Paik, Masaya Miyahara, and Akira Matsuzawa(Tokyo Institute of Technology, Japan)
1J-7	**Modeling of a Double-Sampling Switched-Capacitor Bandpass Delta-Sigma Modulator for Multi-Standard Applications**
11:45	Hong Chang*, Wenxian Lu, Xu Cheng*, Yawei Guo, Xiaoyang Zeng(Fudan University, China)

Thursday, October 27, 10:15 – 12:15 Room 7
Session 2F: Advanced Memory (Ⅱ)

	Title
2F-1	**Challenges and Trends in Low-Power 3D Die-Stacked IC Designs Using RAM, Memristor Logic, and Resistive Memory (ReRAM)(invited paper)**
10:15	Meng-Fan Chang Wei-Cheng Wu, Ching-Hao Chuang(Department of Electrical Engineering, National Tsing Hua University, Hsinchu, Taiwan), Pi-Feng Chiu, Shyh-Shyuan Sheu(EOL, ITRI, Hsinchu, Taiwan)
2F-2	**A 55nm ultra high density two-port register file compiler with improved write replica technique**
10:45	Zhao-Yong Zhang, Yi-Ping Zhang, Rui-Feng Huang, Shou-Dao Wu, Jian-Bin Zheng (Department of Memory Design, AiceStar Technology Corporation, China),Li-Jun Zhang(School of Urban Rail Transportation, Soochow University, China)
2F-3	**Word Line Boost and Read SA PMOS Compensation (SAPC) for ROM in 55nm CMOS**
11:00	Ruifeng Huang1, Jianbin Zheng, Zhaoyong Zhang, Hao Wu, Yue Yu (Aicestar Technology Corp. China),Lijun Zhang(School of Urban Rail Transportation, Soochow University, China)
2F-4	**Design of A Single-Ended Cell Based 65nm 32x32b 4R2W Register File**
11:15	Baoyu Xiong, Xingxing Zhang, Jun Han, Zhiyi Yu, Xiaoyang Zeng(State Key Laboratory of ASIC & System, Fudan University, China)
2F-5	**A 90 nm 16Mb Embedded Phase-Change Memory**
11:30	Hongwei Hong, Zheng Li, Qin Li, Ruizhe Wang(BAMC-BJ Corporation, China), and Charlie Hwang(BAMC, Texas, USA)

Thursday, October 27, 10:15 – 12:15 Room 9

Session 2O: Clock Synthesizer and Building Blocks (Ⅱ)

	Title
2O-2	**A Noise Rejective VCO with Build-in Active LC Filter**
10:45	Ma Zhuo, Guo yang, Xie Lunguo, Liu Rongrong and Zuo Hongjian(*National University of Defense Technology, China*)
2O-3	**A 0.8ps Minimum-Resolution Sub-Exponent TDC for ADPLL in 0.13μm CMOS**
11:00	Xiaolu Liu, Na Yan, Xi Tan, Hao Min(*Fudan University*)

2O-4	**0.5 VDD Digitally Controlled Oscillators Design with Compensation Techniques for PVT Variations**
11:15	Chia-Wen Chang,Shyh-Jye Jou (*National Chiao Tung University, Taiwan*)Yuan-Hua Chu(*Industrial Technology Research Institute, Taiwan*)
2O-5	**Digitally-Controlled Cell-Based Oscillator with Multi-Phase Differential Outputs**
11:30	Ming-Chiuan Su and Shyh-Jye Jou(*National Chiao Tung University, Taiwan R.O.C*)
2O-6	**A 72% Tuning Range Wideband LC-VCO Using Switched Multi-layer Inductors**
11:45	Wanghui Zou, Xiaofei Chen, Dan Wu, Kui Dai, Xuecheng Zou(*Huazhong University of Science and Technology, China*)
2O-7	**A Low Phase Noise Injection-Locked Doubler-based Quadrature CMOS VCO**
12:00	Chen Lian, Wei Li, Haipeng Fu, Ning Li, Junyan Ren (*Fudan University , China*)

Thursday, October 27, 13:30 – 15:30

Thursday, October 27, 13:30 – 15:30 Room 7
Session 1E: Testing, Reliability, Fault-Tolerance (Ⅰ)

	Title
1E-1	**Towards the Next Generation of Low-Power Test Technologies(invited paper)**
13:30	Xiaoqing Wen(Department of Computer Systems and Engineering Kyushu Institute of Technology Japan)
1E-2	**Word Error Control Algorithm through Multi-reading for NAND Flash Memories**
14:00	Chong Zhang(Graduate School of Information, Production and Systems), Tsutomu Yoshihara(Waseda University, Fukuoka, Japan)
1E-3	**A New Scheme for Testability Improvement of ECC Incorporated Memory**
14:15	Lei Wang, Jianhua Jiang , Yumei Zhou, Gaofeng Ren(Institute of Microelectronic Chinese Academy Sciences)
1E-4	**A BIST Scheme for High-speed Gain Cell Edram**
14:30	Bing Yan, Yufeng Xie, Rui Yuan, Yinyin Lin(ASIC & System State Key Lab, Dept.

	of Microelectronics, Fudan University,Shanghai, China)
1E-5	**Variation-Resilient Voltage Generation for SRAM Weak Cell Testing**
14:45	Chingwei Yeh, Yan-Nan Liu, Jinn-Shyan Wang, Pei-Yao Chang(Department of Electrical Engineering, National Chung-Cheng University, Taiwan)
1E-6	**Single Event Upset Immune Latch Circuit Design Using C-Element**
15:00	Ramin Rajaei, Mahmoud Tabandeh , Bizhan Rashidian(Department of Electrical Engineering, Sharif University of Technology, Tehran, IRAN)

Thursday, October 27, 13:30 – 15:30 Room 9 Session 1B: Power Management ICs

	Title
1B-1	**Battery State of Charge Estimation using Adaptive Subspace Identification Method(invited paper)**
13:30	Sahana Swarup, Sheldon X. –D. Tan, Zao Liu, Hai Wang(*University of California, Riverside,USA*), Zhigang Hao, Guoyong Shi(*Shanghai Jiao Tong University, China*)
1B-2	**Design of A Hysteretic-Current-Control Mode LED Driver Based on a 0.6μm BCD Process**
14:00	Lianxi Liu, Zhangming Zhu, Yintang Yang(*Xidian University，China*)
1B-3	**A New Frequency Compensation Scheme for Current-Mode DC/DC Converter**
14:15	Jiake Wang, Jinguang Jiang*, Shanshan Li, Xu Gong, Xifeng Zhou ,Qingyun Li(*Wuhan University , China*)
1B-4	**A High-Performance PWM Controller with Adjustable Current Limit**
14:30	Zekun Zhou, Huifang Wang, Xin Ming, Bo Zhang(*University of Electronics Science and Technology of China, China*),Yue Shi(*Chengdu University of Information Technology, China, University of Electronics Science and Technology of China, China*)
1B-5	**A Capacitor-Free, Fast Transient Response CMOS Low-Dropout Regulator with Multiple-Loop Control**
14:45	Xiao Tang, Lenian He(*Zhejiang University, China*)
1B-6	**A High Efficiency Current Mode Step-Up/Step-Down DC-DC Converter With Smooth Transition**
15:00	Yanzhao Ma, Jun Cheng, Guican Chen(*Xi'an Jiaotong University, China*)

1B-7	**A Non-Rectifier Wireless Power Transmission System Using On-Chip Inductor**
15:15	Yimeng Zhang, Mengshu Huang,Tsutomu Yoshihara(*Waseda University, Japan*)

Thursday, October 27, 13:30 – 15:30 Room 8

Session 1D: Circuits and Systems for Wireless Communications (Ⅰ)

	Title
1D-1	**Wideband Spectrum Sensing using the All-phase FFT(invited paper)**
13:30	Lian Huai, Gerald E. Sobelman(Department of Electrical and Computer Engineering, University of Minnesota, USA),Xiaofang Zhou(State Key Lab of ASIC and System, Fudan University, Shanghai, China)
1D-2	**Low-Complexity Channel Equalization for MIMO OFDM and its FPGA Implementation**
14:00	Tao Xu(Delft University of TechnologyDelft, the Netherlands),Manyi Qian (Beijing Jiaotong University Beijing, China),Rene van Leuken(Delft University of Technology Delft, the Netherlands)
1D-3	**A Robust Frame Synchronization Scheme For Broadband Power-line Communication**
14:15	Chen Chen, Yuebin Huang, Yizhi Wang, Yun Chen, Xiaoyang Zeng(State Key Lab. of ASIC and System, Dept. of Microelectronics, Fudan University Shanghai, China)
1D-4	**FFT Implementation with Multi-Operand Floating Point Units**
14:30	Zhang Zhang1*, Dongge Wang1, Yuteng Pan1, Dan Wang1, Xiaofang Zhou1*, Gerald E. Sobelman2 (*1State Key Lab of ASIC and System, Fudan University, Shanghai 200433, China 2Department of Electrical and Computer Engineering, University of Minnesota, Minneapolis 55455, USA*)
1D-5	**General Lattice Wave Digital Filter with Phase Compensation Scheme**
14:45	Yan Zhao, Jinyuan Zhou, Xiaofang Zhou(*State Key Lab of ASIC and System, Fudan University, Shanghai China*), Gerald E. Sobelman(*Dept. of Electrical and Computer Engineering, University of Minnesota, Minneapolis, USA*)
1D-6	**A High Efficient Baseband Transceiver for IEEE 802.15.4 LR-WPAN Systems**
15:00	Shouyi Yin, Jianwei Cui, Ao Luo, Leibo Liu and Shaojun Wei(Institute of Microelectronics, Tsinghua University National Laboratory for Information Science and Technology Beijing, P.R.China)
1D-7	**System Modeling and Analysis of the IEEE 802.15.4 Physical Layer Design**

15:15	Jikang Xia, Lan Chen, Ying Li, Yinhao Zhou(Institute of Microelectronics, Chinese Academy of Sciences, China)

Thursday, October 27, 15:45 – 17:45

Thursday, October 27, 15:45 – 17:45 Room 9
Session 3R: Wireless transceiver and building blocks (Ⅲ)

	Title
3R-1	**Directional Coupler Design in 3G/LTE Power Amplifier Module(invited paper)**
15:45	Xiao Wang, Wenjun SHeng, Yang Li(*Telink Semiconductor Inc, USA*)
3R-2	**SiGe HBT Power Amplifier Design using 0.35 um BiCMOS Technology with Through-Silicon-Via(invited paper)**
16:15	Jingyang Zhang, Dasheng Fang(*IBM Microelectronics China Design Center, China*), Dawn Wang, Hanyi Ding, John Gillis, Wan Ni, Susan Sweeney(*IBM Microelectronics, USA*)
3R-3	**A Switchable Multi-Band Low Noise Amplifier for Global WiMAX Application**
16:45	Zhe-Yang Huang(*Industrial Technology Research Institute, Taiwan*) Yeh-Tai Hung(*National Chiao Tung University, Taiwan*)
3R-4	**A 0.8-2.5GHz Wideband SiGe BiCMOS Low Noise Amplifier with Noise Fiugre of 1.98-3.3dB**
17:00	Lin Hua, Qiong Yan, Lei Chen,Runxi Zhang, Chunqi Shi, Zongsheng Lai(*East China Normal University , China*)
3R-6	**Design of a High-Linearity RF Front-End With IP2 Calibration for SAW-Less W-CDMA Receiver**
17:15	Song Hu, Weinan Li, Yumei Huang*, and Zhiliang Hong(*Fudan University, China*)

Thursday, October 27, 15:45-17:45 Room 7
Session 1H: CAD for system, Design for Manufacturing and Testing (Ⅰ)

	Title
1H-1	**A New Event Driven Testbench Synthesis Engine for FPGA Emulation**
15:45	Haocheng Huang, Aiwu Ruan, Yongbo Liao, Jianhua Zhu, Lin Wang, Chuanyin Xiang, Pin Li(State key Laboratory of Electronic Thin Films and Integrated Device, University of Electronic Science & Technology of China, China)
1H-2	**An Improved Packing Tool Based on a Dual-Output Basic Logic Element**
16:00	Xianyang Jiang(Institute of Microelectronics and Information Technology, Wuhan University, China), Ying Liu (School of Physics and Technology, Wuhan University, China), Shilei Sun, Gaofeng Wang(Institute of Microelectronics and Information Technology, Wuhan University, China)
1H-3	**A Test Approach of Combining Partial Scan with Functional Testing for High Performance Processors**
16:15	Quanquan Li(Digital System Integration Lab, Institute of Acoustics,Chinese Academy of Sciences, China,and Graduate University of Chinese Academy of Sciences, , China), Yingke Gao, Tiejun Zhang, Chaohuan Hou(Digital System Integration Lab, Institute of Acoustics,Chinese Academy of Sciences, China)
1H-4	**Automatic Layout Generator For Embedded FPGA Cores**
16:30	Chaofan Yu, Lingli Wang, Xuegong Zhou (State-Key-Lab of ASIC and System, Fudan University, Shanghai, China)s
1H-5	**An Optimized Mapping Algorithm Based on Simulated Annealing for Regular NoC Architecture**
16:45	Liulin Zhong, Jiayi Sheng, Ming'e Jing, Zhiyi Yu, Xiaoyang Zeng, Dian Zhou(State Key Laboratory of ASIC&System,Fudan University, Shanghai, China)
1H-6	**The Buildup of FPGA Interconnect Timing Library**
17:00	Xiangzhi Meng, Liguang Chen, Hao Zhou, Jian Wang, Meng Yang, Jinmei Lai(The State Key Lab of ASIC & System, Fudan University, China)

Thursday, October 27, 15:45 – 17:45 Room 8

Session 1R: RF transceiver and building blocks (Ⅰ)

	Title
1R-1	**A 60GHz 16QAM/8PSK/QPSK/BPSK Direct-Conversion Transceiver(invited paper)**
15:45	Kenichi Okada(*Tokyo Institute of Technology, Japan*)
1R-2	**An Area-Efficient Dual-Channel RF Receiver for**

	GPS-L1/Galileo-E1/Compass-B1
16:15	Hongliang Tian, Dongpo Chen, Tingting Mo and Jianjun Zhou(*Shanghai Jiao Tong University, China*)
1R-3	**A 0.8-3GHz 40dB Dynamic Range CMOS Variable-Gain Amplifier**
16:30	Xingli Huang, Xi Qin, Yajie Qin,Zhiliang Hong(*Fudan University, China*),Hao Fang(*LSI Corporation, China*)
1R-4	**A Low-Noise WCDMA Transmitter with 25%-duty-cycle LO Generator in 65nm CMOS**
16:45	Haiyi Wang, Peichen Jiang, Tingting Mo,Jianjun Zhou(*Shanghai Jiao Tong University, China*)
1R-5	**Power Amplifier Driver for SDR Transmitter with High Gain Tuning Range and Dynamic Power Control**
17:00	Yilei Li, Kefeng Han, Na Yan, Xi Tan and Hao Min(*Fudan University, China*)
1R-6	**A 0.18um CMOS 2.5Gbps Pre-Amplifier with AGC**
17:15	Lin Shaoheng(*XIAMEN UX HIGH-SPEED IC CO., LTD, China*)
1R-7	**Aluminum Nitride Reconfigurable RF-MEMS Front-Ends *(invited paper)***
17:30	Augusto Tazzoli*, Matteo Rinaldi*, Chengjie Zuo, Nipun Sinha, Jan Van Der Spiegel, Gianluca Piazza* (University of Pennsylvania, USA)

Thursday, October 27, 15:45 – 17:45 Room 6 Session 2J: Nyquist Analog-to-Digital Converters （Ⅰ）

	Title
2J-1	**A Time-Domain Flash ADC Immune to Voltage Controlled Delay Line Non-Linearity(invited paper)**
15:45	Young-Hwa Kim, and SeongHwan Cho(Korea Advanced Institute of Science and Technology , Korea)
2J-2	**A 10-Bit, 50 MS/s, 55 fJ/conversion-step SAR ADC with Split Capacitor Array**
16:15	Seong-Jin Cho, Yohan Hong, Taegeun Yoo, and Kwang-Hyun Baek (Chung-Ang University, Seoul, Korea)
2J-3	**A 1.8V 100MS/s 10-bit Pipelined Folding A/D Converter With 9.49 ENOB at Nyquist Frequency**
16:45	Xiaojuan Li, Yintang Yang, Zhangming Zhu(Xidian University, China)
2J-4	**A sample-and-hold circuit for 10-bit 100MS/s Pipelined ADC**
17:00	Haitao Wang, Hui Hong, Lingling Sun, and Zhiping Yu(Key Laboratory for

	RF Circuits and Systems of Ministry of Education and Hangzhou Dianzi University, China)
2J-6	**A Low Power 10-bit 100-MS/s SAR ADC in 65nm CMOS**
17:15	Jun Ma, Yawei Guo, Li Li, Yue Wu, Xu Cheng, Xiaoyang Zeng (Fudan University, China)

Thursday, October 27, 17:45 – 18:45

Thursday, October 27, 17:45 – 18:45 Hall

Post Session (II)

	Title
PB01	**TSV Based 3D IC Wire Length Calculation Algorithm**
	Ligang Hou*, Shu Bai, Jinhui Wang(Beijing University of Technology, China)
PB02	**A New Low Power Symmetric Folded Cascode Amplifier by Recycling Current in 65nm CMOS Technology**
	Xiao Zhao, Huajun Fang and Jun Xu(Tsinghua University, China)
PB03	**Ultra low voltage, wide tuning range voltage controlled ring oscillator**
	Li Tianwang1, Jiang Jinguang (Wuhan University Wuhan, China), Ye Bo, Han Xingcheng(Shanghai University of Electric Power, China)
PB05	**A 2.5V Supply Low Noise CMOS Amplifier Using Noise Reduction Technique of Chopper Stabilization**
	Hossein yahyatabar1*, Prof.Farhad Razaghian1, Mehran Yahyavi(Islamic Azad University), Mohsen Habib Nezhad(Multi Media University)
PB07	**Efficient Floating Random Walk Algorithm for Interconnect Capacitance Extraction Considering Multiple Dielectrics**
	Gang Hu, Wenjian Yu(Tsinghua University, China), Hao Zhuang(Peking University, China), Shan Zeng(China University of Geosciences, China)
PB08	**A Dual Mode High efficiency Buck DC-DC Converter**

	Xu Gong, Jinguang Jiang*, Xifeng Zhou (Wuhan University , China)
PB09	**A WiMAX Receiver Front-End for 3.4GHz-3.7GHz Licensed Band Application**
	Zhe-Yang Huang(Industrial Technology Research Institute)
PB10	**A Novel Transimpedance Amplifier for 10 Gbit/s Optical Communication System**
	Taiyi Huang, Qihui Zhang,Weifeng Zhang(Henan University, China)
PB11	**Single Event Upset Mitigation for FDP2008**
	Meng Yang, Gengsheng Chen(Fudan University, China)
PB12	**Electro-thermal Model Extraction of Power GaN HEMT Using I-V Pulsed and DC Measurements**
	Zhifu Hu ,Xuebang Gao, Shujun Cai (Hebei Semiconductor Research Institute ,China)
PB13	**Characterization and Analysis of Pattern dependent Variation-aware Interconnects for a 65nm Technology**
	Lele Jiang, Xiaojing Qin(Shanghai Research Institute of Microelectronics, Peking University, China), Lifu Chang(Semiconductor Manufactuing International Corporation , China), Yuhua Cheng(Shanghai Research Institute of Microelectronics, Peking University, China)
PB14	**Integrated Gm-C Based PI Controller for MEMS Gyroscope Drive**
	Huan-ming Wu, Hai-gang Yang, Xiao-yan Cheng, Tao Yin(Chinese Academy of Sciences, China), Jiwei Jiao(Shanghai Institute of Microsystem and Information Technology, CAS, China)
PB15	**Subthreshold MOSFET Bandgap for Ultra-Low Supply Voltage Yilei Li*, Yu Wang,**
	Na Yan, Xi Tan and Hao Min(Fudan University, China)
PB16	**A Highly Linear Wideband Variable Gain CMOS Balun-LNA**
	Hui Wang, Taotao Yan, Dongpo Chen, and Jianjun Zhou(Shanghai Jiao Tong University, China)
PB17	**A 65nm 10MHz Single-Inductor Dual-Output Switching Buck Converter with Time-Multiplexing Control**
	Miao Yang, Weifeng Sun, Shen Xu, Shengli Lu, Longxing Shi(Southeast University, China)
PB18	**Design and Implementation of pipelined TMVP multiplier using block recombination**
	Xiao Ma1 and Guoqiang Bai (Tsinghua University, China)

PB19	**A Novel Low THD 4-Quadrant Analog Multiplier Using Feedforward Compensation for PFC**
	Yani LI , Yintang YANG , Zhangming ZHU (Xidian University, China), Wei Qiang (Xi'an Longtium Microelectronics Technology Developing Co., Ltd, China)
PB20	**An Inductorless CMOS LNA with Single input and Differential output**
	Jinguang Jiang, Qingyun Li , Xifeng Zhou (Wuhan University, China)
PB21	**A New Nonlinear Parameterized Model Order Reduction Technique Combining the Interpolation Method and Proper Orthogonal Decomposition**
	Zhiyu Xu, Xinnan Lin, Hao Zhuang, Bo Jiang, Haijun Lou (Peking University Shenzhen Graduate School, China), Jin He(PKU HKUST Shenzhen Institute, China)
PB22	**A 0.6 ppm/°C Current-Mode Bandgap with Second-Order Temperature Compensation**
	Yilei Li, Yu Wang, Na Yan*, Xi Tan and Hao Min(Fudan University, China)
PB23	**A 12-bit 50-MSPS SHA-less Opamp-Sharing Analog-to-Digital Converter in 65nm CMOS**
	ChenShu,Guanghua Shu, Jun Xu, Fan Ye, Junyan Ren(Fudan University, China)
PB24	**A Low-Noise Amplifier Using Subthreshold Operation for GPS-L1 RF Receiver**
	Tang Tang, Tingting Mo, and Dongpo Chen(Shanghai Jiao Tong University, China)
PB25	**A sixth-order Chebyshev low-pass filter for single-chip UHF RFID Reader**
	Jiang Chen*, Shilin Zhang, Luhong Mao(Tianjin University, China)
PB26	**A Realizable Reconstruction Filter for Sampled data Systems**
	Muwahida Liaquat, Mohammad Bilal Malik(National University of Sciences and Technology, Pakistan)
PB27	**Optimization of ADM with both restrictions of resolution and power dissipation in low supply voltage**
	Shujuan Yin (Beijing Information Science and Technology University, China), Xiangyu Li(Tsinghua University, China)
PB28	**A Timing-Perspective Study on the Wire Model in Placement**
	Liu Liu (Tsinghua University, China), Yongqiang Lu (Research Institute of Information Technology Tsinghua University, China), Qiang Zhou(Tsinghua University, China)
PB29	**Design for testability of FFT/IFFT IP core for UWB systems**
	Weilu Su1, Longzhao Shi (Fuzhou University, China)

PB30	**A CMOS Hysteresis Undervoltage Lockout with Current Source Inverter Structure**
	Chao Zhang, Zhijia Yang, Zhipeng Zhang (Shenyang Institute of Automation Chinese Academy of Sciences, China)
PB31	**A high linearity MOS capacitor for low voltage applications**
	Shujuan Yin (Beijing Information Science and Technology University, China)
PB32	**A Low-Kickback Preamplifier with Offset Cancellation For Pipelined Folding A/D Converter**
	Xiaojuan Li*, Yintang Yang, Zhangming Zhu (Xidian University, China)
PB33	**Auto-Assign Method for large scale flip-chip package design**
	Haitao Han, Wen Yin, Wenqian Wang, Zegui Pang(IBM GCG Systems & Technology Lab)
PB34	**A 60GHz Power Amplifier using 90-nm RF-CMOS Technology**
	Nan Zhang, Lingling Sun, Jincai Wen, Jun Liu, Jia Lou, Guodong Su, He Li(Hangzhou Dianzi University, China)
PB35	**The Design and Verification of SEU-hardened Configurable DFF**
	Xinrui Zhang, Liguang Chen, Liyun Wang, Jian Wang, Jinmei Lai(Fudan University, China)
PB36	**Efficient Temporal Task Partition for Coarse-Grain Reconfigurable Systems Based on Simulated Annealing Genetic Algorithm**
	Yifan Zhou, Weiguang Sheng, Xie Liu, Weifeng He, Zhigang Mao (Shanghai Jiaotong University, China)
PB37	**Improved Algorithm for Pareto Front Computation for CMOS Opamp Based on Multi-objective Genetic Optimization**
	Peng Chen, Yushun Guo (Hangzhou Dianzi University, China)
PB38	**Calibration Method Considering Second-Order Error Term of Timing Skew for A Novel Multi-Channel ADC**
	Yong-sheng Yin , Rui Zhang, Jun Yang, Ming-lun Gao(Hefei University of Technology, China)
PB39	**12 W/mm, 45% X-band AlGaN/GaN HEMTs on SiC**
	Xinjiang Luo (Hangzhou Dianzi University , China), Zhiguo Zhang Jingqiang Li jianbo Song(China Electronic Technology Group Corporation, China)
PB40	**Large-Signal MOSFET Modeling by Means of Knowledge Based Fuzzy Logic System**

	Liyuan Wang, Yushun Guo (Hangzhou Dianzi University, China)
PB41	**Design and Application of Reusable SoC verification platform**
	Lulu Feng, Zibin Dai, Wei Li, Jianlei Cheng(Zhengzhou Information Science and Technology Institute, China)
PB42	**New power rail ESD clamp design with current starving technology**
	Bo Li, Liji Wu, Xiangmin Zhang (Tsinghua University, China)
PB43	**Design and Implementation of A Low Power Java Coprocessor for dual-interface IC BankCard**
	Junwei He，Liji Wu, Xiangmin Zhang(Tsinghua University, China)
PB44	**A Method to Build Reconfigurable Architectures by Extracting Common Subgraphs**
	Tianyun Zhang, Rui Zhang, Lingli Wang(Fudan University, China), Yu Hu(University of Alberta, Canada)
PB45	**A novel high-accuracy clock stabilizer with 50% duty cycle**
	Biye Xu, Lenian He(Zhejiang University, China)
PB46	**A 1.2 V 70 mA Low Drop-out Voltage Regulator in 0.13 μm CMOS Process**
	Qin Wu, Wei Li, Ning Li, Junyan Ren(Fudan University, China)
PB47	**Compensator Design for Digital Controlled Switched-Mode Power Supplies**
	Ling Lin, Jianping Qiu, Lenian He(Zhejiang University, China)
PB49	**A 1.2-V 250-MS/s 8-bit Pipelined ADC in 0.13-μm CMOS**
	Peiyuan Wan, Wei Lang, Di Fang, Wei Cui, and Pingfen Lin(Beijing University of Technology, China)
PB50	**A Novel RSD Correction for Pipeline ADC**
	Dawei Fu, Lenian He, Biye Xu(Zhejiang University, China)
PB51	**A Digital Sliding Mode controller for Swiching Power Supply Converters**
	Guannan Xu, Chen Jia, Chun Zhang, Zhihua Wang (Tsinghua University, China)
PB52	**A Low-Power Gm-R-C Image Rejection Filter for Complex Low-IF Receiver**
	Hao Li, Hong Zhang, Xunwei Weng, Ruizhi Zhang (Xi'an Jiaotong University, China)
PB53	**A 4GS/s 3b Two-way Time-Interleaved ADC in 0.13um CMOS**

	Cunchen Gu, Yi Zhao, Zhiliang Hong(Fudan University, China)
PB54	**A Low Power 1.0 GHz VCO in 65nm-CMOS LP-Process**
	Zhang Zhang (Hefei University of Technology, China), Zhiyi Yu, Xu Cheng, Xiaoyang Zeng (Fudan University, China)
PB55	**Three Stage Low Noise Operational Amplifier in 0.18 um CMOS**
	Saber Izadpanah Tous*, Abbas Golmakani(Sadjad University, IRAN)
PB56	**A Charge-Pump Circuit to Restrain Reference Spurs in the PLL**
	Changhong Huan, Xiushan Wu(China Jiliang University, China), Dan Wang (Anhui University of Technology, China)
PB57	**A Wide Lock-Range, Low Jitter Phase-Locked Loop for Multi-Standard SerDes Application**
	Shaolong Liu , Hui Wang, Yuhua Cheng(Shanghai Research Institute of Microelectronics, Peking University, China)
PB58	**Ultralow-power Analog Front-End IC Design for an Implantable Cardioverter Defibrillator (ICD) (invited paper)**
	Weibo Hu[1], Yen-Ting Liu[1], Tam Nguyen[1,2], Bosco Dsouza[1] and Donald Y.C. Lie[1,2] (*1Texas Tech University (TTU), USA. 2Texas Tech Health Sciences Center (TTUHSC), USA*)

Friday, October 28, 10:15 – 12:15

Friday, October 28, 10:15 – 12:15 Room 7 Session 2H: CAD for system, Design for Manufacturing and Testing (Ⅱ)

	Title
2H-1	**Robustness and Performance analysis on High Speed ASIC design with canonical statistical timing model**
10:15	Suoming Pu, Bo Yu, Xuan Zou(China Design Center, IBM Microelectronics, China)
2H-2	**Optimization of Mixed Polarity Reed-Muller Expressions Based on Whole Annealing Genetic Algorithm**
10:30	Meng Yang(State Key Lab of ASIC & System, Fudan University , China), Hongying Xu(Tianjin Vocational College of Mechanics and Electricity, China)
2H-3	**CPIPQ: A Common Platform for Silicon IP Qualification**
10:45	Mark P. C. Mok, Kenneth C. K. Lo, Yuzhong Jiao, Yiu Kei Li(IC Design Group, Hong Kong Applied Science and Technology Research Institute (ASTRI), Hong Kong)
2H-4	**Comprehensive Electro-Thermal(ET) Analysis with Considering ET coupling**
11:00	Huang Kun, Zhao Guoxing, Yang Xu, Luo Zuying(College of Information Science and Technology, Beijing Normal University, China)
2H-5	**Latency-Aware Mapping for 3D NoC Using Rank-Based Multi-Objective Genetic Algorithm**
11:15	Jiawen Wang, Li Li*, Hongbing Pan, Shuzhuan He, Rong Zhang(Institute of VLSI Design, Nanjing University, China Key Laboratory of Advanced Photonic and Electronic Materials, Nanjing University, China)
2H-6	**Mobility Overlap-Removal Based Timing-Constrained Scheduling**
11:30	Song Chen, Yuan Yao, and Takeshi Yoshimura(Graduate School of Information, Production, and Systems, Waseda University, Japan)
2H-7	**An Effecient Level-shifter Floorplanning Method for Multi-Voltage Design**
11:45	Xiaolin Zhang, Zhi Lin, Song Chen, Takeshi Yoshimura

Friday, October 28, 10:15 – 12:15 Room 6 Session 1K: New Processing & Devices, Hetro-integration, 3-D integration (Ⅰ)

	Title
1K-1	**Novel Flash Ion Sensitive Field Effect Transistor for Chemical Sensor**

	Applications(invited paper)
10:15	Chao-Sung Lai(Department of Electronic Engineering, Chang Gung University,Taiwan,and Biosensor Group, Biomedical Engineering Center, Chang Gung University, Taiwan),Tseng-Fu Lu(Department of Electronic Engineering, Chang Gung University,Taiwan),Jer-Chyi Wang(Department of Electronic Engineering, Chang Gung University,Taiwan,and Biosensor Group, Biomedical Engineering Center, Chang Gung University, Taiwan)
1K-2	**A Model for Energy Quantization of Single-electron Transistor Below 10nm**
10:45	Xiaobao Chen, Zuocheng Xing, Bingcai Sui(School of Computer, National University of Defense Technology, China)
1K-3	**An Efficient Design Algorithm for Exploring Flexible Topologies in Custom Adaptive 3D NoCs for High Performance and Low Power**
11:00	Xin Jiang, Ran Zhang and Takahiro Watanabe(Graduate School of Information, Production & Systems, Waseda University, Japan)
1K-4	**LDO based Design and Optimization of Power Distribution under Worst Performance**
11:15	Amirali Shayan, Xiang Hu, Chung-Kuan Cheng(epartment of Computer Science and Engineering University of California, San Diego La Jolla, CA)

Friday, October 28, 10:15 – 12:15 Room 8
Session 1N: Other VLSI Device and Design related topics

	Title
1N-1	**Physics-Based Compact Variability/Reliability Modeling for Emerging Double-Gate/Nanowire MOSFETs(invited paper)**
10:15	Xing Zhou (*Nanyang Technological University, Singapore*)
1N-5	**Performance Evaluation Modeling for Reconfigurable Processor**
11:30	Shuang Liang*, Shouyi Yin, Chongyong Yin, Leibo Liu, Shaojun Wei(Tsinghua University, China)

1N-7	**A High Performance Clock Precharge SEU Hardened Flip-flop**
12:00	Riadul Islam, S.E. Esmaeili(Department of Electrical & Computer Engineering, Canada), Thouhidul Islam(Department of Electrical & Electronic Engineering, Bangladesh University of Engineering & Technology,Bangladesh)
1N-8	**Design of 2-3 mixed-valued/six-valued adiabatic asynchronous up-down counter**
12:15	Fengna Mei(Institute of Circuits and Systems, Ningbo University, China), Pengjun Wang(State Key Laboratory of ASIC & System, Fudan University, China)

Friday, October 28, 10:15 – 12:15 Room 9
Session 2B: Analog Techniques (Ⅰ)

	Title
2B-1	**An Overview of Charge Pumping Circuits for Flash Memory Applications(invited paper)**
10:15	Oi-Ying Wong, Hei Wong*, Wing-Shan Tam, and Chi-Wah Kok(*City University of Hong Kong, Hong Kong*)
2B-2	**Class-AB CMOS buffer with floating class-AB control**
10:45	Peng Zhang, Fan Ye,Junyan Ren(*Fudan University, China*)
2B-3	**Programmable Fuzzifier Circuits with High Precision for Analog Neuro-Fuzzy System**
11:00	Habib Ghasemizadeh Tamar,Aghil Ahmadi, Abdollah Khoei,Khayrollah Hadidi(*Urmia Microelectronic Research Laboratory, Iran*)
2B-4	**A New Topology for Fully Differential Amplifiers that Enhances Their Tolerance to External Disturbances**
11:15	Guoyuan Fu[1]*, H. Alan Mantooth[1], Jia Di(*University of Arkansas, Fayetteville, USA*)
2B-5	**Three-Stage Amplifier with Recycling Folded Cascode Input-Stage and Active-Capacitive Feedback Techniques**
11:30	Qianneng Zhou, Min Tan(*National Labs of Analog Integrated Circuit, China*), Hongjuan Li,Rong Xue, Zhe Wang(*Chongqing University of Posts and Telecommunications, China*)
2B-6	**Double charge pump circuit with triple charge sharing clock scheme**

11:45	Mengshu Huang, Yimeng Zhang, Hao Zhang ,Tsutomu Yoshihara(*Waseda University, Japan*)
2B-7	**CMOS Charge Pump with Separated Charge Sharing for Improved Boosting Ratio and Relaxed Timing Restriction**
12:00	Seung-Jae Choi(*Sungkyunkwan University, Korea, Samsung Electronics, Korea*) Young-Hyun Jun(*Samsung Electronics, Korea*), Bai-Sun Kong(*Sungkyunkwan University, Korea*)

Friday, October 28, 13:30 – 15:30

Friday, October 28, 13:30 – 15:30 Room 9
Session 3B: Analog Techniques for Sensor Signal Conditioning

	Title
3B-2	**ROIC with Adaptive Reset Control for Improving Dynamic Range of IR FPAs(invited paper)**
13:30	Doohyung Woo(*The Catholic University of Korea, Korea)*, Ilku Nam, Joonwoo Choi(*Pusan National University, Korea*)
3B-3	**A Signal Conditioner IC for Inductive Proximity Sensors**
14:00	Huang Wengang(*SISC, China, UESTC, China*), Wang Chenghe, Liu Luncai, Huang Xiaozong, and Wang Guoqiang(*SISC, China*)
3B-4	**A Low-power Low-noise Amplifier for EEG/ECG Signal Recording Applications**
14:15	Jinghao Feng,Na Yan,Hao Min(*Fudan University, China*)
3B-6	**A TIA-based Interface for MEMS Capacitive Gyroscope**
14:30	Tao Yin, Huanming Wu, Qisong Wu, Haigang Yang(Chinese Academy of Sciences, China), Jiwei Jiao(*CAS, China*)

Friday, October 28, 2011, 13:30 – 15:30 Room 8
Session 1C: Application-Specific SoCs (Ⅰ)

	Title

1C-1	**A Multi-level Arbitration and Topology Free Streaming Network for Chip Multiprocessor(invited paper)**
13:30	Jian Wang, Andreas Karlsson, Joar Sohl, Magnus Pettersson , Dake Liu(Department of Electrical Engineering Link¨oping University, Sweden)
1C-2	**Design and Verification of an Application-Specific PLD Using VHDL and SystemVerilog(invited paper)**
14:00	Jae-Jin Lee(Electrionics and Telecommunications Reaserch Institute, Deajeon, Korea), Young-Jin Oh, Gi-Yong Song(School of Electronics engineering College of Electrical and Computer Engineering, Korea)
1C-3	**Evaluation of Deflection Routing on Various NoC Topologies**
14:30	Chaochao Feng, Jinwen Li, Minxuan Zhang(School of Computer, National University of Defense Technology, China) ,Zhonghai Lu, Axel Jantsch(Department of Electronic Systems, Royal Institute of Technology, Sweden)
1C-4	**ASIC Implementation of an OFDM Baseband Transceiver for HINOC**
14:45	Hongming Chen(Shanghai Research Institute of Microelectronics (SHRIME), Peking University, China), Xiaoyuan Chen, Tie Liu , Yuhua Cheng(Shanghai Bwave Technology Co., Ltd Shanghai, China)
1C-5	**Design of Four-Transistor Pixel for High Speed CMOS Image**
15:00	Zhou Yangfan, Cao Zhongxiang, Li Quanliang, Qin Qi, Wu Nanjian(State Key Laboratory for Superlattices and Microstructures, Institute of Semiconductors, Chinese Academy of Sciences,China)
1C-6	**A Network-on-Chip Simulation Framework for Homogeneous Multi-Processor System-on-Chip**
15:15	Yuan Wen Hau, M. N. Marsono, Chia Yee Ooi, M. Khalil-Hani(VeCAD Research Laboratory Faculty of Electrical Engineering, Universiti Teknologi Malaysia.Malaysia.)

Friday, October 28, 13:30 – 15:30 Room 7

Session 1G: Circuits Simulation, Synthesis, Verification and Physical design (Ⅰ)

	Title
1G-1	**Separate Projection and Extended Cauer Method for Circuit Reduction(invited paper)**
13:30	Goro Suzuki(University of Kitakyushu JAPAN)
1G-2	**VLSI Interconnect Delay Analysis Method for Ramp Input Signal(invited paper)**

14:00	Nobuyuki Mihara,Goro Suzuki(University of Kitakyushu JAPAN)
1G-3	**RRA-Based Multi-Objective Optimization to Mitigate the Worst Cases of Placement**
14:30	Yiqiang Sheng, Shuichi Ueno(Department of Communication and Integrated Systems Tokyo Institute of Technology, Japan),Atsushi Takahashi(Division of Electrical, Electronic and Information Engineering Osaka UniversityJapan)
1G-4	**Numerical Characterization of Multi-Dielectric Green's Function for Floating Random Walk Based Capacitance Extraction**
14:45	Hao Zhuang(Department of Computer Science and Technology, Tsinghua University, China, and School of Electronics Engineering and Computer Science, Peking University, China), Wenjian Yu, Gang Hu(Department of Computer Science and Technology, Tsinghua University, China), Zuochang Ye(Institute of Microelectronics, Tsinghua University, China)
1G-5	**Power Grid Sizing via Convex Programming**
15:00	Peng Du, Shih-Hung Weng, Chung-Kuan Cheng(CSE Dept.), Xiang Hu(ECE Dept., University of California, San Diego, CA)
1G-6	**Polarity optimization of XNOR/OR circuit area and power based on weighted sum method**
15:15	Huihong Zhang(Institute of Circuits and Systems, Ningbo University, China), Pengjun Wang(Institute of Circuits and Systems, Ningbo University, China ,and State Key Laboratory of ASIC & System, Fudan University, China)

Friday, October 28, 13:30 – 15:30 Room 6

Session 2K: New Processing & Devices, Hetro-integration, 3-D integration (Ⅱ)

	Title
2K-1	**A Unipolar-CMOS with Recessed Source/Drain Load(invited paper)**
13:30	Jyi-Tsong Lin, Hsuan-Hsu Chen, Kuan-Yu Lu, Chih-Hung Sun(Department of electrical engineering, National Sun Yat Sen University, Taiwan ROC) Tung-Yen Lai, Fu-Liang Yang(National Nano Device Laboratories , Taiwan)
2K-2	**An analytical model for SOI triple RESURF devices**
14:00	Haimeng Huang, Yongwei Wang, Xingbi Chen(State Key Laboratory of Electronic Thin Films and Integrated Devices University of Electronic Science and Technology of China, China)
2K-3	**A Study of Second Saturation Effect of OPTVLD NMOS**
14:15	Wenfang Du, Xingbi Chen(State Key Laboratories of Electronic Thin Films and

	Integrated Devices University of electronic science and technology of China, Chengdu, China)
2K-4	**Quantum Mechanical Effects on the Threshold Voltage of the Evenly Doped Surrounding-Gate MOSFETs**
14:30	Guanghui Mei, Peicheng Li, Guangxi Hu, Ran Liu, Tingao Tang(State Key Lab of ASIC and System, School of Information Science and Technology,Fudan University, China)
2K-5	**Effect of Structural Parameters on the Performance and Variations of Nanosizes PNIN Tunneling Field Effect Transistor**
14:45	S. Q. Cheng, C. J. Yao, D. M. Huang(State Key Laboratory of ASIC and System, Department of Microelectronics, Fudan University, China)
2K-6	**Exploring 3D Power Distribution Network Physics**
15:00	Xiang Hu(ECE Dept). , Peng Du, Chung-Kuan Cheng(CSE Dept., University of California, La Jolla, CA)
2K-7	**An Efficient Solver for Statistical Capacitance Extraction Considering Random Process Variations**
15:15	Rubing Bai(Department of Computer Science and Technology, Tsinghua University, China), Shan Zeng(School of Software, China University of Geosciences, Beijing, China), Qingqing Zhang(Department of Computer Science and Technology, Tsinghua University, China,and College of Information Science and Technology, Beijing Normal University, China), Wenjian Yu(Department of Computer Science and Technology, Tsinghua University, China)

Friday, October 28, 15:45 – 17:45

Friday, October 28, 15:45 – 17:45 Room 9
Session 3J: Nyquist Digital-to-Analog Converters

	Title
3J-1	**A Dual 12bit 80MSPS 3.3V Current-Steering DAC for HINOC Application**
15:45	Hongming Chen ,Yuhua Cheng(Shanghai Research Institute of Microelectronics, Peking University, China), Xiaoyuan Chen(Shanghai Bwave Technology Co., Ltd)
3J-2	**A 4-Channel 8-bit 650-MSample/s DAC with Interpolation Filter for Embedded Application**

16:00	Qianqian Ha, Fan Ye, Chixiao Chen, Xiaoshi Zhu, Mingshuo Wang, Yujing Lin, Ning Li,Junyan Ren(Fudan University, China)
3J-3	**A New Current Switch Driver with Improved Dynamic Performance Used for 500MS/s, 12-bit Nyquist Current-Steering DAC**
16:15	Guojia Liu, Lenian He , Xiaobo Xue, Qifeng Shi(Zhejiang University, China)
3J-4	**A 14-Bit 2-GSs DAC with SFDR 70dB up to 1-GHz in 65-nm CMOS**
16:30	Ran Li, Qi Zhao, Ting Yi, Zhiliang Hong(Fudan University, China)
3J-5	**A Multi-mode 1-V DAC+filter in 65-nm CMOS for Reconfigurable (GSM, TD-SCDMA and WCDMA) Transmitters**
16:45	Li Li, Jun Ma, Yawei Guo, Xu Cheng, Xiaoyang Zeng(Fudan University, China)

Friday, October 28, 15:45-17:45 Room 6
Session 1I: MEMS technology, device and circuits

	Title
1I-1	**Survey of Resistor Geometric Variation in multi-bridge Absorptive Capacitive Shunt MEMS Switch(invited paper)**
15:45	Hamidreza sayyar, khalil kafinezhad(Sadjad Institute for Higher Education, Mashhad, Iran)
1I-2	**The Manufacturing of Si Base Thin Film Solar Cell Modules(invited paper)**
16:15	Tingkai Li(Hunan Gongchuang Photovoltaic Science & Technology Co., Ltd., China)
1I-3	**Challenges and Strategies in Advanced CMOS Technology Development(invited paper)**
16:45	Xiaomeng Chen(Semiconductor Research and Development Center, Microelectronics Division, IBM, USA)
1I-4	**Research on electromechanical model of micro-accelerometer based on SOI technology**
17:15	Keqiang Qian , Wen Luo, Qi Yu(State Key Lab of Electronic Thin Films and Integrated Devices, Univ. of Electronics Science & Technology of China China)
1I-5	**CMOS Compatible MEMs Process for Post Interconnect Single Chip Integration Application**
17:30	Xiaoxu Kang, Qingyun Zuo, Jiaqing Li, Chao Yuan, Yuhang Zhao(Process Technology Department, Shanghai IC R&D Center, China)

Friday, October 28, 15:45-17:45	Room 8
Session 2C: Application-Specific SoCs (Ⅱ)	

	Title
2C-1	**Design of a Signal Processing Circuit for Quartz Crystal Microbalance Biosensors(invited paper)**
15:45	Shih-Chang Chang(Department of Electrical Engineering, National University of Tainan, Taiwan), I-Jen Chao, Bin-Da Lin(Department of Electrical Engineering, National Cheng Kung University, Taiwan), Chun-Yueh Huang(Department of Electrical Engineering, National University of Tainan, Taiwan), Mei-Hwa Lee(Department of Materials Science and Engineering, I-Shou University, Taiwan), Hung-Yin Lin(Department of Chemical and Materials Engineering, National University of Kaohsiung, Taiwan)
2C-2	**A Low-power 433MHz Transmitter for Battery-less Tire Pressure Monitoring System**
16:15	inyu Zhu, Liji Wu, Xiangmin Zhang, Chen Jia, Chun Zhang(Tsinghua National Laboratory for Information Science and Technology Institute of Microelectronics, Tsinghua University, Beijing. China)
2C-3	**A High Performance and Low Cost Video Processing SoC for Digital HDTV Systems**
16:30	Longjun Liu, Hongbin Sun, Wenzhe Zhao, Zuoxun Hou, Jingmin Xin, Nanning Zheng(School of Electronics and Information Engineering, Xi'an Jiaotong University, China)
2C-4	**A Novel Hardware Prefetching Scheme Exploiting 2-D Spatial Locality in Multimedia Applications**
16:45	Jin Huang, Jing Xie, Zhigang Mao(School of Microelectronics, Shanghai Jiao Tong University, China Building of Microelectronics, China)
2C-5	**A NoC-based Multi-core Architecture for IEEE 802.11i CCMP**
17:00	Yang Li, Jun Han, Shuai Wang, Junbao Liu and Xiaoyang Zeng(State-Key Lab of ASIC and System, Fudan University, China)
2C-6	**A Method of Quadratic Programming for Mapping on NoC Architecture**
17:15	Jiayi Sheng, Liulin Zhong, Ming'e Jing, Zhiyi Yu, Xiaoyang Zeng(State Key Laboratory of ASIC & System, Fudan University, Shanghai, China)
2C-7	**A Channel Estimator for LTE Downlink Mapped on a Multi-Core Processor Platform**

17:30	Maofei He, Jiajie Zhang, Wenhua Fan, Zhiyi Yu, Xiaoyang Zeng(State Key Lab of ASIC and System, Fudan University, P.R.China)

Friday, October 28, 15:45-17:45 Room 7

Session 2G: Circuits Simulation, Synthesis, Verification and Physical design (Ⅱ)

	Title
2G-1	**Don't Let the X-Bugs Bite: Conquer Elusive X-Propagation Issues Early!Get Them Before They Get You!(invited paper)**
15:45	Lisa Piper, Jin Zhang(Real Intent, Inc, Sunnyvale, CA)
2G-2	**Meshim：A High-Level Performance Simulation Platform for Three-Dimensional Network-on-Chip**
16:15	Menwang Xie(University of Science and Technology of China, China), Duoli Zhang(Hefei University of Technology , China), Yao Li(University of Science and Technology of China, China)
2G-3	**Through-Silicon-Via Assignment for 3D ICs**
16:30	Jianchang Ao, Sheqin Dong(Department of Computer Science and Technology, Tsinghua University, Beijing, China), Song Chen, Satoshi Goto(Graduate School of IPS, Waseda University, Kitakyushu-shi, Japan)
2G-4	**Incremental layout optimization for NoC Designs Based on MILP Formulation**
16:45	Jia Liu,Yuchun Ma(Department of Computer Science and Technology, Tsinghua University, China) Ning Xu(School of Computer Science and Technology, WuHan University of Technology, China),Yu Wang(Department of Electronic Engineering, Tsinghua University, China)
2G-5	**Standard Cell Design of a Low-Leakage Flip-Flop**
17:00	Jianping Hu,Jun Wang(Faculty of Information Science and Technology, Ningbo University , China)
2G-6	**Debugging Methodology and Timing Analysis in CDC Solution**
17:15	Akitoshi Matsuda(Kyushu Embedded Forum,Japan), Jin Zhang(Technical Marketing, Real Intent, USA)
2G-7	**Circuit Simulation by Matrix Exponential Method**
17:30	Shih-Hung Weng, Quan Chen, Chung-Kuan Cheng(Department of Computer Science and Engineering, University of California, San Diego, CA)

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ASICON 2011 Technical Program Overview

Date	Time	Sea-view Meeting Rooms 6	Sea-view Meeting Rooms 7	Sea-view Meeting Rooms 8	Sea-view Meeting Rooms 9	
Oct.25 Tue。	AM 9:00	Tutorial Session T1 & T2	Tutorial Session T5			
	PM 2:00	Tutorial Session T3 & T4				
Oct.26 Wed。	8:30—10:00	Opening & Keynote Session K1 (International Auditorium)				
	10:15-12:15	Keynote Session K2 & K5 (International Auditorium)				
	13:30-15:30	Session 4J: Reference & Nyquist Analog-to-Digital Converters (Ⅱ)	Session 1F: Advanced Memory (Ⅰ)	Session 1A: VLSI Design and Circuits (Ⅰ)	Session 2R: Wireless transceiver and building blocks (Ⅱ)	
	15:45-17:45	Special Session: ESL Design	Session 2E: Testing, Reliability, Fault-Tolerance (Ⅱ)	Session 2A: VLSI Design and Circuits (Ⅱ)	Session 1O: Clock Synthesizer and Building Blocks (Ⅰ)	
	17:45-18:45	Poster Session 1 (Hall)				
	19:00-21:00	Reception				
Oct.27 Thu。.	8:30-10:00	Keynote Session K3 & K4 (International Auditorium)				
	10:15-12:15	Session 1J: Analog Filters and Oversampling Data Converters	Session 2F: Advanced Memory (Ⅱ)	Session 3A : VLSI Design and Circuits (Ⅲ)	Session 2O: Clock Synthesizer and Building Blocks (Ⅱ)	
	13:30-15:30		Session 1E: Testing, Reliability, Fault-Tolerance (Ⅰ)	Session 1D : Circuits and Systems for Wireless Communications (Ⅰ)	Session 1B: Power Management ICs	
	15:45-17:45	Session 2J: Nyquist Analog-to-Digital Converters (Ⅰ)	Session 1H: CAD for system, Design for Manufacturing and Testing (Ⅰ)	Session 1R: RF transceiver and building blocks (Ⅰ)	Session 3R: Wireless transceiver and building blocks (Ⅲ)	
	17:45-18:45	Poster Session 2 (Hall)				

Oct.28 Fri。.	10:15-12:15	Session 1K: New Processing & Devices, Hetro-integration, 3-D integration (Ⅰ)	Session 2H: CAD for system, Design for Manufacturing and Testing (Ⅱ)	Session 1N : Other VLSI Device and Design related topics	Session 2B: Analog Techniques (Ⅰ)	
	13:30-15:30	Session 2K: New Processing & Devices, Hetro-integration, 3-D integration (Ⅱ)	Session 1G: Circuits Simulation, Synthesis, Verification and Physical design (Ⅰ)	Session 1C : Application-Specific SoCs (Ⅰ)	Session 3B: Analog Techniques for Sensor Signal Conditioning	
	15:45-17:45	Session 1I: MEMS technology, device and circuits	Session 2G: Circuits Simulation, Synthesis, Verification and Physical design (Ⅱ)	Session 2C : Application-Specific SoCs (Ⅱ)	Session 3J: Nyquist Digital-to-Analog Converters	
	19:00-21:00	Banquet				

Introduction of Conference Site

Xiamen

Xiamen, the second largest city in Fujian province next to the capital Fuzhou, covers a total area of 1,516 square meters. As one of the five earliest special economic zones, with heavy investment from Taiwan and Hong Kong, it has been a city growing in strength.

Despite its fame as an industrial powerhouse, this port city has not lost much of its charm, and as a sightseeing haven has become one of the best areas to visit in Fujian and for good reason: With good food, some great architecture and a mild to hot climate, Xiamen is hard to beat.

Xiamen International Seaside Hotel

Located at picturesque Island Ring Road scenic spot, 5-star International Seaside Hotel, is one of members of Xiamen Jianfa Tour Group. It is only 4,600m away from Taiwan's Big and Little Quemoy Islands across the straits, and connected with Xiamen International Conference & Exhibition Center via a long glass-porch. The Hotel is designed with overwhelmingly exceptional style, seeming like a ready-to-sail luxurious cruise staying put at the southeast coast of China. With its total length of 325m, it is worthy of the Longest Hotel in the World.

Being accessible to the hotel, it is only 15 minutes' ride from Xiamen Gaoqi International Airport, 20 minutes' from the rail station, and 25 minute's from the ferry .

The International Seaside Hotel possesses 208 guest rooms, including 131 sea-view guest rooms with the area of more than 50 m2 each, which are the most capacious and comfortable ones in the southeast coastal area, enabling you to enjoy fabulous sunrise and sunset as well as pleasure brought by gentle sea breeze on the super panoramic sea-view balcony, which is very close to the Taiwan's Big and Little Quemoy Islands.

Each room is equipped with broadband Internet access available to facilitate and speed up your business. The Housekeeping Center has prepared variety of comfortable pillows such as buckwheat-stuffed pillow and down-stuffed pillar to ensure your sweet sleep.

The Hotel possesses 10 well-equipped conference venues, and armed with a team with profound experience and professional quality in conferencing. Including a International Auditorium capable of accommodating over 400 audience, and a 800 ㎡ Koron Banquet Hall accommodating over 500 audience. The Hotel shares 28 banquet/conference venues with the neighboring International Conferences & Exhibition Center, of which the multi-function hall, the biggest of its kind in Xiamen, enables to accommodate up to 2000 audience.

The Seaside Cafeteria & Lounge, located at lobby of the Hotel, is the best place for leisure, enabling you to savor gourmet as well as to feast your eyes on beautiful sea view. Meanwhile, you can be indulged in top coffee's refreshment and culture content in the fashionable and comfortable Nebur-King Coffee Porch. The French Byland Oyster Bar, elegant and luxurious, offers French cuisine mainly featuring top-grade fresh oysters, allowing you to savor romance of French's style. The Larruping Bay Chinese Restaurant, simple and elegant, features the neo-Cantonese Cuisine, Min Cuisine, Jiaodong Cuisine and Xiamen Seafood, with 10 sea-view VIP rooms available. The Ginzar Bar in Japanese style offers Japanese wine and other kinds of wine.

2,000 m2 Tianxin Club, the biggest foot-bath city in Xiamen, features services such as foot-bath, body-building, sauna, dry steaming, as well as recreational services such as KTV, Chess & Card and billiards.

In the International Seaside Hotel, where you can go for a walk and fly kite on 150,000 m2 green seaside lawn, or feast your eyes on the sea view while jogging along the seaside, or ride on a duo-bicycle for pleasant travel in sea breeze along the most graceful marathon race track in the world.
The Hotel joined the Golden Key Hotels of The World on Jan. 19, 2004. The Hotel was three times awarded as The Top 10 Popular Resort Hotels and China Gold Key Service Diamond & 5C Quality Award in China from 2005 to 2007 for its advantaged environment and high quality service.

Tour Information

- 1 DAY Xiamen Highlight Tour, Price From:$ 105p.p.
- 1 Day Yongding Earthen Building Tour, Price From:$ 102 p.p.
- 2 Days Yongding Earthen Building & Peitian Ancient Village Tour, Price From:$ 195 p.p.
- 3 Days Fairlyland Mt. Wuyishan Private Tour, Price From:$ 455 p.p.

For the details, please visit our website:
www.discoverchinatours.com/destinations/xiamen-tours.htm

Location of Conference Hotel

ASICON 2011 FINAL PROGRAM

DATE AND VENUE

Oct. 25-28, 2011
Xiamen International Seaside Hotel
Xiamen, China

Sponsor:	*IEEE Beijing Section* *Fudan University*
Co-Sponsors:	*IEEE China Council* *Xiamen University, China* *IEEE SSCS Shanghai Chapter* *IET Beijing Branch*
Technical Co-Sponsors:	*IEEE-CAS* *IEEE-SSCS* *Chinese Institute of Electronics (CIE)*
Supporters:	*National NSF of China*
Organizer	*Fudan University*

Hotel Prospect Photo