ASICON 2009

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2009 8th IEEE International Conference on ASIC

October 20-23, 2009

Changsha, China

Edited by **Ting-Ao Tang**

Xiaoyang Zeng

Yun Chen

Huihua Yu

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Welcome to ASICON 2009

On behalf of the Organizers of the Conference, it is my great pleasure and honor to express our warm welcome to all ASICON 2009 attendees. Thank you very much for your great support to come to Changsha under the influence of global financial crisis.

ASICON 2009 is the 8 th event of this conference series. The conference will be held from October 20 to 23, 2009 at Preess Resort & Hotel, Changsha, China. The conference is intended to provide an international forum for VLSI circuit designers, ASIC users, System Integrators, IC manufacturers and CAD/CAE tool developers to present their updated progresses, developments and research results in their respective fields. The Conference is also intended to afford a platform for attendees to exchange academic and technical information.

This time, we have received all together 552 papers from 16 countries and areas. After serious paper review process by more than 90 experts, 160 oral papers and 40 invited papers have been accepted by the TPC of ASICON 2009 which will be presented in 35 technical sessions.

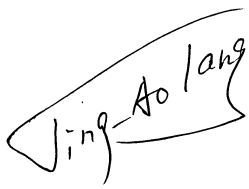
Conforming to the consuetude of international conference, ASICON 2009 organizes some famous experts to give seven tutorials on the first day. The topics of those tutorials are all research hot points about IC design. Additionally, we are very pleased to have invited 6 worldwide famous professors and enterprisers to give brilliant Keynote speeches on the plenary sessions from Oct.21-23.

The conference has traditionally a strong impact on both industries and academia. We do hope the peculiar tradition can be strengthened and carried forward through this conference.

This is the second time for ASICON to be held other than Beijing and Shanghai. Changsha is a very beautiful city. We sincerely hope all of you will have a good time in Changsha.

General Chair of ASICON 2009

Ting-Ao Tang



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[1]Berkeley Design Automation, United States; [2]University of California, Riverside, United States

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Wang Rui, Wang Gaofeng
Wuhan University, China

7F-4 **The Minimum Delay Calculation Methods in Hybrid Timing Analysis**
Zhentao Li, Jihua Chen, Shuming Chen, Yao Liu
National University of Defense Technology, China

7F-5 **Random Walk Algorithm for Large Thermal RC Network Analysis**
Jun Guo[1], Sheqin Dong[1], Satoshi Goto[2]
[1]Tsinghua University, China; [2]Waseda University, Japan

SESSION 7G

Industrial Low-Power Design Methodologies

7G-1 **A proposal for a capture method of low power design intent**
Yoshio Inoue
EDA Methodology Group Manager, Renesas Technology Corp., Japan

7G-2 **Power Aware Design for Next Generation's Many cores Computing Platforms**
Roberto Zafalon
STMicroelectronics, Switzerland

7G-3 **Advances in CAD for Low Power Design**
Martin D.F. Wong
University of Illinois at Urbana-Champaign

SESSION 8A

Nano Devices Technology

8A-1 **Multi-Gate-Length versus Dual-Gate-Length Biasing for Active Mode Leakage Power Reduction: Benchmarking and Modeling**
Qiang Chen, Sridhar Tirumala
Synopsys, United States

8A-2 **Geometry Optimization of SiGe HBTs for Noise Performance of the Monolithic Low Noise Amplifier**
Pei Shen, Wanrong Zhang, Hongyun Xie, Dongyue Jin

Beijing University of Technology, China

8A-3 **A Novel Dual SCR Device for ESD Protection**
Bo Yu, Yuan Wang, Song Jia, Ganggang Zhang
Peking University, China

8A-4 **Quantum-Mechanical Study on the Electron Effective Mobility of Surrounding-Gate nMOSFETs**
Guang-Xi Hu, Ran Liu, Ting-Ao Tang, Ling-Li Wang, Zhi-Jun Qiu
Fudan University, China

8A-5 **VLSI Design of Resource Shared Complex-QMF Bank for HE-AAC Decoder**
Junqiao Huang, Gaoming Du, Duoli Zhang, Yukun song, Luofeng Geng, Minglun Gao
Hefei University of Technology, China

SESSION P1

Poster Session (I)

1P-1 **An Efficient Verification and Test Scheme for HDTV Demodulator**
Yun Chen, Nan Shao, Bo Xiang, An Pan, Xiaoyang Zeng
Fudan university, China

1P-2 **A High-Throughput Cost-Effective ASIC Implementation of the AES Algorithm**
Qingfu Cao, Shuguo Li
Tsinghua University, China

1P-4 **A Fast-lock Digital Delay-Locked Loop Controller**
Bo Ye[1], Tianwang Li[2], Xingcheng Han[3], Min Luo[4]
[1]Shanghai University of Electric Power, China; [2]Wuhan University, China; [3]Integrated Silicon Solution(Shanghai) Co.,Ltd., China; [4]Lucent Technologies Optical Networks Co.,Ltd., China

1P-5 **Performance Evaluation of the Memory Hierarchy Design on CMP Prototype Using FPGA**
Yan Liu[1,2], Li Dongsheng[1], Zhang Duoli[1], Du Gaoming[1], Wang Jian[2], Gao Minglun[1], Wen Haihua[1], Geng Loufeng[1]
[1]Hefei University of Technology, China; [2]East China Institute of Photo-Electronic, China

1P-6 **Power-aware FPGA Packing Algorithm**
Meng Yang[1], Hongying Xu[2], A.E.A. Almaini[3]
[1]Fudan University, China; [2]Tianjin Vocational College of Mechanics and Electricity;

[3]Napier University

1P-7 **High Computing-Intensive Array System Design and Hardware Implement**
Yukun Song, Xiaolei Wang, Wei Ni, Duoli Zhang, Gaoming Du
Hefei University of Technology, China

1P-8 **Tradeoff Design for Analog Integrated Circuits via Geometric Programming**
Dan Li, Guo Hua Shu, Meng Tian Rong
Shanghai Jiao Tong University, China

1P-9 **Clocked Storage Elements Robust to Process Variations**
Joosik Moon, Mustafa Aktan, Vojin G. Oklobdzija
University of Texas at Dallas, United States

1P-10 **Research and Implementation of Parallel and Reconfigurable MICKEY Algorithm**
LI Miao, XU Jinfu, DAI Zibin, YANG Xiaohui, QU Hongfei
Zhengzhou Information College, China

1P-11 **A Power and Area Efficient Architecture of Convolver Based on Ram**
Chen Chen, Yun Chen, Yuan Chen, An Pan, Xiao-Yang Zeng
Fudan University, China

1P-12 **A Design of level Interface of CMP based Cache System**
Chen Chen, Hu He, Yuan Liu
Tsinghua University, China

1P-13 **Scalable and Unified Hardware Architecture for Montgomery inverse in GF(p) and GF(2n)**
Yang Xiao-hui, Qin Fan, Dai Zi-bin, Zhang yong-fu
Information Engineering University, China

1P-14 **Design and Optimization on Reconfigurable Butterfly Core for a Real-Time FFT Processor**
Zhizhe Liu, Shunan Zhong, Yueyang Chen, Weinan Chu
Beijing Institute of Technology, China

1P-15 **Design of Low-Power Complementary Pass-Transistor and Ternary Adder Based on Multi-valued Switch-signal Theory**
Xiaopang Zeng, Pengjun Wang
Ningbo University, China

1P-16 **A Look-Up-Table Based Differential Logic to Counteract DPA Attacks**

Daheng Yue, Yan Sun, Minxuan Zhang, Shaoqing Li, Yutong Dai
National University of Defense Technology, China

1P-17 **A Parallel Intra Prediction Architecture for H.264 Video Decoding**
Xi WANG, Xiaoxin CUI, Dunshan YU
Peking University, China

1P-18 **DM-SIMD: A New SIMD Predication Mechanism for Exploiting Superword Level Parallelism**
Libo Huang, Li Shen, Sheng Ma, Nong Xiao, Zhiying Wang
National Unviersity of Defense Technology, China

1P-19 **A 1Gsample/Sec Non-Recursive Sharpened Cascaded Integrator-Comb Filter with 70 dB alias rejection and 0.003 dB droop in 0.18- m CMOS**
Xiong LIU, Alan N. WILLSON, JR.
University of California, Los Angeles, United States

1P-20 **Trade-offs in the Design of a Universal Sensor Interface**
Qi Jia, Xiujun Li, Gerard C.M. Meijer
Delft University of Technology, Britain

1P-21 **Design and Implementation of Configurable Extract Instructions targeted at Stream Cipher Processing**
Longmei Nan, Zibin Dai, Wei Li, Xueying Zhang, Zhongxiang Chang
Zhengzhou Institute of Information Technology, China

1P-22 **Single-Phase Adiabatic Flip-Flops and Sequential Circuits with Power-Gating Scheme**
Haiyan Ni, Jianping Hu
Ningbo University, China

1P-23 **Design of Ternary Adiabatic T-operation Circuit Based on the Theory of Three Essential Circuit Elements**
Kunpeng Li, Pengjun Wang
Ningbo University, China

1P-24 **Least Operation Traversal Method Applied in Optimization of Logic Circuits**
Huihong Zhang[1], Pengjun Wang[1], Xingsheng Gu[2], Jing Dai[1]
[1]Ningbo University,China; [2]East China University of Science and Technology, China

1P-25 **High Performance and Low Latency Mapping for Neural Network into Network on Chip Architecture**
Yiping Dong, Yang Wang, Zhen Lin, Takahiro Watanabe

Waseda University, Japan

1P-26 **An improved edge-adaptive image scaling algorithm**
Wen Jiang, Haifeng Xu, Gengsheng Cheng, Wenqing Zhao, Wei Xu
Fudan University, China

1P-27 **A Data-flow Graph Generation Algorithm for a Coarse-grained Reconfigurable Processor**
Chao Yang, Shouyi Yin, Leibo Liu, Shaojun Wei
Tsinghua University, China

1P-28 **Data Compression and the 8x8 Integer Transform**
Min. Zhu, Wen Jia, Leibo Liu, Shaojun Wei
Tsinghua University, China

1P-29 **A Weighted Statistical Analysis of DPA Attack on an ASIC AES Implementation**
Guoyu QIAN[1], Ying ZHOU[1], Yueying XING[1], Yibo FAN[1], Yukiyasu TSUNOO[2], Satoshi GOTO[1]
[1]Waseda University, Japan; [2]NEC Corporation, Japan

1P-30 **Design and Implementation of Dynamic Distance Sensor Using MATLAB and GUIDE**
Hemnath S
National Institute of Technology, Tiruchirappalli, India

1P-31 **Efficient Hardware IP Control and Simulation with LabVIEW**
Taewan Kim, Yunmo Chung
KyungHee University, Korea

1P-32 **A Novel Architecture of Vision Chip for Fast Traffic Lane Detection and FPGA Implementation**
YuanJin Li, WanCheng Zhang, NanJian Wu
Chinese Academy of Sciences, China

1P-33 **CMOL Cell Assignment Based on Dynamic Interchange**
Zhufei Chu, Yinshui Xia, Lunyao Wang, Meiqun Hu
Ningbo University, China

1P-34 **A 2.4GHz Non-Contact Biosensor System for Continuous Vital-Signs Monitoring on a Single PCB**
Ravi Ichapurapu[1], Suyash Jain[1], Donald Y.C. Lie[1], Mandar U Kakade[1], Ronald E. Banister[2]
[1]Texas Tech University, United States; [2]Texas Tech Health Sciences Center, United States

1P-35 **A Technique of Data Streams Speculation for Heterogeneous MC-DSPs**

Wang Dong, Chen Shuming
National University of Defense Technology, China

1P-36 **Power Analysis Resistant AES Crypto Engine Design and FPGA Implementation for a Network Security Co-processor**

Yingjie Ji, Liji Wu, Xiangmin Zhang, Xiangyu Li
Tsinghua University, China

1P-37 **Blind Separation Algorithm for Microphone Array Based on Recursive Neural Network**

Fan Jiajun, Fu Yuzhuo, Liu Ting
Shanghai Jiaotong University, China

1P-38 **Neural Signal Electronics Bridge Integrated Circuit**

Gao Liu, Wenyuan Li, Zhigong Wang
Southeast University, China

1P-39 **Design and Experimental Research on Shallow Water Volume Reverberation Signal Acquisition System**

Yongwei LIU, Qi LI, Mengying CHEN
Harbin Engineering University, China

1P-40 **Architectural integration of RSA Accelerator into MIPS processor**

Shiting Lu, Suiyu Zhang, Yulong Zhang, Jun Han, Xiaoyang Zeng
Fudan University, China

1P-41 **Quality of Service Routing Algorithm in the Torus-based Network on Chip**

Kun Wang, Changshan Wang, Huaxi Gu
Xidian University, China

1P-42 **A Switched Hall IC for Automotive Electronic Applications**

Dongfang Cheng, Zhifei Yi, Weiyong Wang, Xiaohui Li
Shanghai University, China

1P-43 **Integrated CMOS Amplifier with DC Rejection Scheme for Sensor Application**

Jinyong Zhang[1], Bin Li[1], Lei Wang[2]
[1]South China University of Technology, China; [2]Shenzhen Institutes of Advanced Technology, China

1P-44 **Design of On-chip Image Processing Based on APB Bus with CMOS Image Sensor**

Ge Zhiwei, Yao Suying, Xu Jiangtao

Tianjin University, China

1P-45 **Automatic Parallelization Experiments on 16PE NOC Based MPSOC**

Tian, Hammami

École Nationale Supérieure de Techniques Avancées (ENSTA), France

1P-46 **Design and FPGA Implementation of JAVA CARD Coprocessor for EMV Compatible IC Bankcard**

Di WU, Liji WU, Xiangmin ZHANG

Tsinghua University, China

1P-47 **A Low-Cost Custom HF RFID System for Hand Washing Compliance Monitoring**

Suyash Jain[1], Shashank Mane[1], Jerry Lopez[1], Donald Y.C. Lie[1], Tim Dallas[1], Sharmila Dissanaike[2], Ronald E. Banister[2], John Griswold[2]

[1]Texas Tech University, United States; [2]Texas Tech University Health Sciences Center, United States

1P-48 **A Joint Mode Detection and Coarse Symbol Synchronization Scheme for DVB-H**

Zewen Shi, Yulong Zhang, Yan Ying, Xiaoyang Zeng

Fudan University, China

1P-49 **An UHF RFID Transponder for ISO 18000-6B**

Xiaoxing Feng, Xin'an Wang, Xing Zhang, Binjie Ge, Jinpeng Shen, Shan Liu, Yongzhen Qi, Jinsi Zhong

Peking University Shenzhen Graduate School, China

1P-50 **A New DOA Estimation Method for Uncorrelated and Coherent Sources under Nonstationary Noise Fields**

Yiduo Guo, Yongshun Zhang, Ningning Tong

Missile Institute of Air Force Engineering University, China

1P-51 **A Novel Programmable Ultra-Wideband Transmitter**

DengHongLin, Zhang Sheng, Quan Jinguo, Liu Meng-meng, Lin Xiaokang

Tsinghua University, China

1P-52 **An Multi-Rate LDPC Decoder Based on ASIP for DMB-TH**

Xiaojun Zhang[1], Yinghong Tian[1], Jianming Cui[1], Zongsheng Lai[1], Yuyin Xu[2]

[1]East China Normal University, China; [2]Shangdong University of science and Technology, China

1P-53 **Design and Implementation of a Security-Enhanced Baseband System for UHF RFID Tag**

Qi Yongzhen, Wang Xin'an, Feng Xiaoxing, Gu Weqing

Shenzhen Graduate School of Peking University, China

1P-54 **Low-Complexity Architecture of RS Decoder for CMMB System**
Kun Guo, Yong Hei, Shushan Qiao
Chineses Academy of Sciences, China

1P-55 **A Cost efficient LDPC decoder for DVB-S2**
Yan Ying, Dan Bao, Shuangqu Huang, Bo Xiang, Xiaoyang Zeng, Yun Chen
Fudan University, China

1P-56 **High-reliable multi-level Phase Change Memory with Bipolar Selectors**
Le Xu, Yufeng Xie, Yinyin Lin
Fudan University, China

1P-57 **A Pure Logic CMOS Based Low Power Non-Volatile Random Access Memory for RFID Application**
Yaru YAN, Dong WU, Huijuan Liu, Liyang PAN, Jun XU
Tsinghua University, China

1P-58 **Flow field plate of micro fuel cell fabrication in UV-nanoimprint lithography**
Si Weihua[1], Liu Zewen[1], Dong Xiaowen[2], Gu Wenqi[2]
[1]Tsinghua University, China; [2]Chinese Academy of Sciences, China

1P-59 **Thermal Stress Analysis of The Microtoroid Under CO_2 Laser**
Guoqing Jiang, Shubin Yan, Yingzhan Yan, Jijun Xiong
North University of China, China

1P-60 **Improved Thermal Stability of Power SiGe Heterojunction Bipolar Transistor with Novel Emitter Structure**
Ning Hu, Wan-rong Zhang, Liang Chen, Lu Huang, Yi-wen Huang
Beijing University of Technology, China

1P-61 **Investigation into Trap-assisted Tunneling Drain Leakage Current in NMOSFETs**
Xing Dezhi[1], Liu Hongxia[2], Li Kaicheng[3]
[1]National Labs of Analog Integrated Circuits and Sichuan Institute of Solid-state Circuits, China; [2]Xidian University, China; [3]Sichuan Institute of Solid-state Circuits, China

1P-62 **An Experimental Extracted Model for Latchup Analysis in CMOS Process**
Ye Li[1], Xiaohan Gong[1], Weiwei Xu[1], Zhiliang Hong[1], Dirk Killat[2]
[1]Fudan University, China; [2]Brandenburg University of Technology, German

1P-63 **A Novel MTJ-based Register**

Yanfeng Jiang, Xiaobo Zhang, Jiaxin Ju
North China University of Technology, China

1P-64 **Effect of refractive index of dielectric on transmission properties for metal/dielectric/metal photonic crystal**
Gongli Xiao[1,2], Yiping Huang[1], Zongming Bao[1]
[1]Fudan University, China; [2]Guilin University of Electronic Technology

1P-65 **The Gate-Bias Influence for ESD Characteristic of NMOS**
Juan Liu, Hang Fan, Jianguo Li, Lingli Jiang, Bo Zhang
University of Electronic of Electronic Science and Technology of China, China

1P-66 **The Size Optimize of DCVSPG Logic**
Yuanbin Xie, Weitao Pan, Peijun Ma, Yue Hao
XiDian University, China

1P-67 **Negative Differential Regime free LIGBT utilizing Resistance-Controlled-Anode**
Gang Xie, Wensuo Chen, Bo Zhang, Zhaoji Li
University of electronic science and technology of China, China

SESSION P2

Poster Session (II)

2P-1 **Development and Production of ZCS Soft Switching Converter-based Gate Driver IC**
Jun Jiang, Xian Wu, Bo Hu, Jianjun Liao, Lu Zhao
Sichuan Institute of Solid-state Circuit, China

2P-2 **A High Efficiency Filter-less Class-D Audio Power Amplifier**
Yu-Jei Lin[1], Wan-Rone Liou[1], Mei-Ling Yeh[2]
[1] National Taipei University, Taiwan; [2] National Taiwan Ocean University, Taiwan

2P-3 **A Synchronous Boost Regulator with PWM/PFM Mode Operation**
Wan-Rone Liou, Ping-Hsing Chen, Jiun-Chang Tzeng
National Taipei University, Taiwan

2P-4 **A Low Spur Charge Pump In 0.35 m SiGe Process for PLL**
Song Ye[1], Lingling Wu[2], Yang Yu[2], Xuan Wu[2], Shuailin Zhou[2], Shoulong Tang[2]
[1]Chengdu University, China; [2]Broad Galaxy Electronics Technology Inc, China

2P-5 **A Sub-1V 115nA 0.35 m CMOS Voltage Reference for Ultra Low-Power Applications**
Haifeng MA, Feng ZHOU

Fudan University, China

2P-6 **2.4 GHz Doherty Power Amplifier with on-chip Active Balun Design**
Mei-Guang Li, Qi-Rong Wu, Rui-Ying Shi
Sichuan University, China

2P-7 **Digital Static Calibration Technology Used for 16-bit DAC**
Zhu Dongmei[1], Fu Dongbing[1], Shi Jiangang[1], Li Kaicheng[2]
[1]National Labs of Analog Integrated Circuits, China; [2]Sichuan Institute of Solid-state Circuits, China

2P-8 **A Novel 0.72-6.2GHz Continuously-Tunable û Fractional-N Frequency Synthesizer**
Wenfeng Lou, Xiaozhou Yan, Zhiqing Geng, Nanjian Wu
Chinese Academy of Sciences, China

2P-9 **A Low Dropout Regulator with Over current reminder Circuits**
Wang Yong-sheng, Li Rui-xuan, Yu Ming-yan, Lai Feng-chang
Harbin Institute of Technology, China

2P-10 **A sample/hold circuit for 80MSPS 14-bit A/D converter**
XIAO Kun-guang, WANG Yu-Xing, XU Min-Yuan, Zhu Chan
National Laboratory of Analog Integrated Circuits, China

2P-11 **Single-Inductor Dual-Output Converter with Dynamic Power Distribution**
Yueming Sun, Xiaobo Wu, Menglian Zhao
Zhejiang University, China

2P-12 **CCCII and CCII Based Universal Current-mode Filter with Tunable Frequency**
Jinguang Jiang, Jing Zhao, Wei Ma, Jingnan Liu
Wuhan University, China

2P-13 **A Simple Parameter Extraction Method for On-Chip Inductors**
Xiaoming Lu, Jingtian Xi, Na Yan, Hao Min
Fudan University, China

2P-14 **A novel building block: universal current conveyor**
Zhang Qiujing, Wang Chunhua, Leng Yang
Hunan Univesity, China

2P-15 **A Low Power Self-Sampling IF FSK Receiver**
Yang Xu, Baoyong Chi, Zhihua Wang
Tsinghua University, China

2P-16 **A Nonlinear Phase Frequency Detector for Fast-Lock Phase-Locked Loops**

Jinbao Lan, Fengchang Lai, Zhiqiang Gao, Hua Ma, Jianwei Zhang
Harbin Institute of Technology, China

2P-17 **A Parallel-Amplification Parallel-Summation Logarithmic Amplifier for UHF RFID Reader**

Yong Zhang, lei Chen, Xiaojun Zhang, Zongsheng Lai
East China Normal University, China

2P-18 **Design of Parallel Backlight LED Driver IC**

JaeHyung LEE[1], LiYan JIN[1], LongZhen LI[2], PanBong HA[1], YoungHee KIM[1]
[1]Changwon National University, Korea; [2]YanBian University, China

2P-19 **Design of Compensation Circuits for Quasi-Resonant PWM Controllers**

Zhao Ye[1], Zhou Yumei[1], Duan Liye[2]
[1]Chinese Academy of Sciences, China; [2]Hunan University, Chinese Academy of Sciences, China

2P-20 **A Constant-Gain Time-Amplifier with Digital Self-Calibration**

Baoli Tong, Wei Yan, Xiaofang Zhou
Fudan University, China

2P-21 **A 2.4-GHz Low-IF Front-end Receiver in 0.18-μm CMOS for IEEE 802.15.4 WPAN Applications**

Bao-lin WEI, Yu-jie DAI, Xiao-xing ZHANG, Ying-jie LU
Nankai University, China

2P-22 **An Ultra Low Power Sigma-Delta Modulator for Hearing Aid with Double-Sampling**

Da Qi, Yuan-wen Li, Long Cheng, Jun Xu, Fan Ye, Jun-yan Ren
Fudan University, China

2P-23 **A 760mV CMOS Voltage Reference with Mobility and Subthreshold Slope Compensation**

Yongjia Li, Xiaojuan Xia, Weifeng Sun, Shengli Lu
Southeast University, China

2P-24 **Process-Insensitive General Purpose Rail-to-Rail Operational Amplifier Using Unity-Size Transistors**

Shengqi Yang[1], Fuding Ge[2]
[1]Shanghai University; [2]Intel Corporation, United States

2P-25 **Design of a 2.5Gbps Clock-Data Recovery circuit in 0.18um standard CMOS process**

Chen Yueyang, Zhong Shun'an, Dang Hua
Beijing Institute of Technology, China

2P-26 **A Method of Weak Signal Detection Based on Duffing Oscillator**

Chu-lin Hou, De-shi Wang
Naval University of Engineering, China

2P-27 **A Novel Fast-Settling ADPLL Architecture with Frequency Tuning Word Presetting and Calibration**

Weicheng Zhang, Xuan Dai, Jing Jin, Jianjun Zhou
Shanghai Jiao Tong University, China

2P-28 **Design of Novel Bootstrap Driver Used in High Power BUCK Converter**

Zekun Zhou, Xing Ming, Bo Zhang, Zhaoji Li
University of Electronic Science and Technology of China, China

2P-29 **Design of a Noise-canceling Differential CMOS LNA for 3.1-10.6 GHz UWB Receivers**

Liu Jinhua, Chen Guican, Ruizhi Zhang
Xi'an Jiaotong University, China

2P-30 **True Single-Phase Energy Recovery Flip-Flop for Low-Power Application**

Leisheng Gao, Yumei Zhou, Hainan Liu
Chinese Academy of Sciences, China

2P-31 **A 200MHz Low-Power Direct Digital Frequency Synthesizer Based on Mixed Structure of Angle Rotation**

Wan Shuqin[1], Huang Yiding[2], Zhang Kai-hong[3], Yu Zongguang[3]
[1]Jiangnan University, China; [2]Nanyang Normal University, China; [3]China Electronics Technology Group Corporation No. 58 Research Institute, China

2P-32 **0.5 V 1.3 GHz voltage controlled ring oscillator**

Tianwang Li[1], Bo Ye[2], Jinguang Jiang[1]
[1]Wuhan University, China; [2]Shanghai University of Electrical Power, China

2P-33 **A Zero-ESR Stable Adaptively Biased Low-dropout Regulator in Standard CMOS Technology**

Min Tan
Integrated Circuit design center, SISC, CETC, Chongqing, China

2P-34 **Design of 16-bit 400MSPS Current Steering D/A Converter**

Fu Dongbing[1], Zhu Dongmei[1], Zhou Shutao[2], Li Kaicheng[2]

[1]National Labs of Analog Integrated Circuits, China; [2]Sichuan Institute of Solid-state Circuits, China

2P-35 **Practical Tuning of an OTA-C Bandpass Biquad via Recurrent Geometric Programming**

Roungsan Chaisricharoen, Boonruk Chipipop
Mae Fah Luang University, Thailand

2P-36 **Stochastic Inductance Model of OTA-based Inductor**

Rawid Banchuin, Rougsan Chaisrichatorn, Boonruk Chipipop
Siam University, Thailand

2P-37 **Design of Common Gate UWB LNA in CMOS**

Li Cai, Zongqian Fu, Lu huang
University of Science and Technology of China, China

2P-38 **Battery-less Piezoceramics Mode Energy Harvesting for TPMS**

Liji WU, Yixiang WANG, Chen JIA, Chun ZHANG
Tsinghua University, China

2P-39 **Novel Method of Analog Circuit Schematic Synthesis**

Yuping Wu
Chinese Academy of Science, China

2P-40 **A Jitter Measurement Circuit Based On Dual Resolution Vernier Oscillator**

Wei Tang[1], Jianhua Feng[1], Chunglen Lee[2]
[1]Peking University, China; [2]National Chiao Tung University, Taiwan

2P-41 **Multi-classifier Fusion Approach based on Data Clustering for Analog Circuits Fault Diagnosis**

Song Guoming, Wang Houjun, Liu Hong, Jiang Shuyan
University of Electronic Science and Technology of China, China

2P-42 **Hierarchical SoC Testing Scheduling Based on the Ant Colony Algorithm**

Xiaole Cui[1], Wei Cheng[1], Xiaoye Wang[1], Liang Yin[1], Yachun Sun[2], Yan Zhou[2]
[1]Shenzhen Graduate School of Peking University, China; [2]Shenzhen National Integrated Circuit Industrial Center

2P-43 **Novel TSC CMOS Circuit**

KIM JEONG BEOM
Kangwon National University, Korea

2P-44 **Full Coverage Location of Logic Resource Faults in A SOC Co-Verification Technology Based FPGA Functional Test Environment**

Y.B.Liao, P.Li, A.W.Ruan, W.Li, W.C.Li
University of Electronic Science and Technology of China, China

2P-45 **Power Noise Analysis Acceleration Technique by Linear Programming**

Goro Suzuki, Takeshi Gomakubo
University of Kitakyushu, Japan

2P-46 **Effectiveness Analysis of Low Power Technique of Dynamic Logic under Temperature and Process Variations**

Jinhui Wang[1], Wuchen Wu[1], Na Gong[2], Wang Zhang[1], Ligang Hou[1]
[1]Beijing University of Technology, China; [2]Hebei University, China

2P-47 **Variation RLC Model of Interconnect Based on Weibull Distribution**

Jianwei Li, Yintang Yang, Gang Dong, Zeng Wang
Xidian University, China

2P-48 **Surface-Potential-Based Analysis of Bias-Dependent Series Resistance in LDD MOSFET**

Lei Chen, Lingling Sun, Jun Liu
Hangzhou Dianzi University, China

2P-49 **DCCB and SCC Based Fast Circuit Partition Algorithm For Parallel SPICE Simulation**

Xiaowei Zhou, Yu Wang, Huazhong Yang
Tsinghua University, China

2P-50 **An Improved Resource Allocation Algorithm for Testability**

Sun Qiang
Mudanjiang Teachers College, China

2P-51 **Architecture of SystemC based Emulator for ReMAP**

Lai Wei, Peng Dai, Xi'an Wang, Yanliang Liu
Peking University, Shenzhen Graduate School, China

2P-52 **The verification of the substrate mathematics model and Optimization of the substrate noise Canceling Technique in mixed signal ICs**

Dongfang Cheng, Wenrong Yang, Jiongming Wang
Shanghai University, China

2P-53 **Multi-Voltage and Level-Shifter Assignment Driven Floorplanning**

Bei Yu[1], Sheqin Dong[1], Satoshi GOTO[2]
[1]Tsinghua University, China; [2]Waseda University, Japan

2P-54 **A New Electrothermally-Aware Methodology for Full-Chip Temperature Optimization**
Gang Dong, Peng Leng, Changchun Chai, Yintang Yang
Xidian University, China

2P-55 **Design of SoC Verification Platform Based on VMM Methodology**
Lu Kong, Wu-Chen Wu, Yong He, Ming He, Zhong-Hua Zhou
Beijing University of Technology, China

2P-57 **Transistor Permutation for Better Transistor Chaining**
Xun Chen[1], Jianwen Zhu[2]
[1]National University of Defence Techenology, China; [2]University of Toronto, Canada

2P-58 **Convex-cost Flow based Redundant-Via Insertion with Density-Balance Consideration**
Wei Guo, Song Chen, Mei-Fang Chiang, Jian-Wei Shen, Takeshi Yoshimura
Waseda University, Japan

2P-59 **Design and Implementation of MCU Chip for Automobile TPMS**
Bin Xiao, Liji Wu, Chen Jia, Chun Zhang
Tsinghua University, China

2P-60 **Formal Verification of Mixed-signal Circuits using Extended PSL**
Meng Zhang, Deyuan Gao, Xiaoya Fan
Northwestern Polytechnical University, China

2P-61 **Pin Assignment for Wire Length Minimization after Floorplanning Phase**
Xu He, Sheqin Dong
Tsinghua University, China

2P-62 **Congestion-driven Floorplanning based on Two-stage Optimization**
Fubing Mao[1], Ning Xu[1], Yuchun Ma[2], Yu Wang[2], Xianlong Hong[2]
[1]WuHan University of Technology; [2]Tsinghua University, China

2P-63 **Template-based Compilation for Coarse-grained Reconfigurable Processor**
Shouyi YIN, Chongyong YIN, Leibo LIU, Shaojun WEI
Tsinghua University, China

2P-64 **Formal Verification of Full-Wave Rectifier: A Case Study**

Kusum Lata, H S Jamadagni
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2P-65 SystemVerilog-based Verification Environment using SystemC Custom Hierarchical Channel

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