

2017 IEEE 12th International Conference on ASIC



ASICON 2017

Final PROGRAM

Oct. 25-28, 2017

Pullman Hotel, Guiyang, China





**2017 IEEE 12th
International
Conference on ASIC**

ASICON 2017

**Oct. 25-28, 2017
Pullman Hotel, Guiyang, China**

Sponsored by

*IEEE Beijing Section
Fudan University
Technical Sponsor IEEE CASS*

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*IEEE SSCS Shanghai Chapter
IET Shanghai Network
Chinese Institute of Electronics (CIE)*

Organized by

Fudan University

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Welcome to ASICON 2017

On behalf of the Conference, it is my great pleasure and honor to express our warm welcome to all ASICON 2017 attendees. Thank you very much for your participation.

ASICON 2017 is the 12th event of this conference series that began in 1994. The Conference will be held from Oct. 25 to 28, 2017 at Pullman Hotel, Guiyang, China. Guiyang is a beautiful historical city. We sincerely hope that you will have a rewarding and good time in Guiyang.

While “ASIC” has had a narrow meaning, the Conference has adopted **A**dvanced **S**emiconductor **I**ntegrated **C**ircuits as the meaning of **ASIC** in ASICON. This normally recognizes the fact that ASICON covers all the technical fields of integrated circuits. The conference provides an international forum for VLSI circuit designers, ASIC users, System Integrators, IC manufacturers and CAD/CAE tool developers to present their new progresses, developments and research results in their respective fields. The Conference also affords a platform for academic and industry attendees to network and exchange information.

ASICON 2017 has invited international experts to give tutorials on the first day of the conference. In addition, we have invited 7 world renowned academic and industry leaders to give keynote speeches on the plenary sessions from Oct. 26-28.

ASICON has a strong positive impact on industry and academia. We look forward to continuing this tradition with you this year.

General Co-Chairs of ASICON 2017

2017.10

Conference Committee

General Co-Chairs

Name	Affiliation	Country/Area
Chenming Hu	UC Berkeley	USA
Ting-Ao Tang	Fudan University	China
Jan Van der Spiegel	University of Pennsylvania	USA
Richard.M.M. Chen	IEEE HK Section	Hongkong
Satoshi Goto	Waseda University	Japan
Yong Lian	York University	Canada

Advisory Committee Co-Chairs

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Omar Wing	Columbia University	USA
Qianling Zhang	Fudan University	China
Hiroshi Iwai	Tokyo Institute of Technology	Japan

Program Committee Co-Chairs

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Bin Zhao	Fairchild	USA
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Yajie Qin	Fudan University	China

Technical Program Committee Members of ASICON 2017

Analog and RF Circuits Subcommittee		
Chen, Weizen	National Chiao Tung University	Taiwan
Li, Qiang	University of Electronic Science and Technology of China	China
Sai Weng Sin	University of Macau	Macao
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Song, Fei	MediaTek Inc	USA
Wu, Nanjian	Institute of Semiconductor, CAS	China
Zhang, Wenjun	Intel Corp.	USA
Ye, Fan	Fudan University	China
Zhou, Jianjun	Shanghai Jiaotong University	China
Huang, Yumei	Fudan University	China
Zhao, Dixian	Southeast University	China
Cheng, Lin	Hongkong University of Science and Technology	Hongkong
Lu, Zhenghao	Suzhou University	China
Yu, Xiaopeng	Zhejiang University	China
Killat, Lng.Dirk	Brandenburg University of Technology Cottbus	Germany
Piero Malcovati	Universita Degli Studi Di Pavia	Italy
Han, Ruonan	Massachusetts Institute of Technology	USA
Tian, Tong	Chinese Academy of Sciences	China
Gao, Yuan	Institute of Microelectronics	Singapore
Zhang, Feng	Institute of Microelectronics, Chinese Academy of Sciences	China
Digital Circuits and Systems Subcommittee		
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Wang, Shaoyun	NextInput Inc.	Canda
Zhang, Chuan	Southeast University	China

Chacko John Deepu	National University of Singapore	Singapore
Gerald E.Sobelman	University of Minnesota	USA
Gong, Na	North Dakota State University	USA
Liu, Liang	Lund University	Sweden
Makoto Ikeda	University of Tokyo	Japan
Wang, Jinhui	Beijing University of Technology	China
Wu, An-Yeu	National Taiwan University	Taiwan
Yu, Zhiyi	SYSU-CMU Joint Institute of Engineering	China
Zhou, Dajiang	Waseda University	Japan
Zhang, Tong	Rensselaer Polytechnic Institute	USA
Hao San	Tokyo City University	Japan
Wang, Guoxing	Shanghai Jiao Tong University	China
Huang, Mo	Institutes Of Technology Of South China	China
EDA Techniques, Devices and Process Subcommittee		
Li, Xiaowei	Institute of Computing Technology, CAS	China
Tan, Sheldon X. D.	University of California, Riverside	USA
Shi, Weiping	Texas A&M University	USA
Shi, Youhua	Waseda University	Japan
Yu, Wenjian	Tsinghua University	China
Hou, Ligang	Bejing University of Technology	China
Lin, Yinyin	Fudan University	China
Gao, Jianjun	East China Normal University	China
Geng, Li	Xi'an jiaotong University	China

General Information

● Conference Language

The official language is English. No simultaneous translation is available.

● Conference Schedule

Date	Time	Event
Oct. 25	AM & PM	Tutorial Session & Registration
Oct. 26	AM	Opening & Keynote Session
		Keynote Session (K1-1,K1-2, K1-3)
	PM	Parallel Sessions
		Parallel Sessions
		Poster Session (1)
Evening	Reception	
Oct. 27	AM	Keynote Session (K2-1,K2-2)
		Parallel Sessions
	PM	Parallel Sessions
		Poster Session (2)
Oct. 28	AM	Keynote Session (K3-1,K3-2)
		Parallel Sessions
	PM	Parallel Sessions
		Parallel Sessions
Evening	Banquet	

● Conference Site

The conference will be held in **Hotel Pullman Guiyang**

Tel: (+86)851/8866668 Fax: (+86)851/8866669

Add: No.100 Jie Fang Road, Nanming District, Guiyang, China

Website: <http://www.pullmanhotels.com/gb/hotel-8275-pullman-guiyang/index.shtml>

● Conference Registration

Payment by Credit Card, Bank Transfer, or Check

1. **Participant:** Accepted Paper ID Number(if available): _____

Mr. Ms. First Name: _____ Last Name: _____

Affiliation (Univ./Company): _____

Address: _____

Phone: _____ Mobile: _____ Email: _____

2. Registration Fee

Classification	Before Sep.15, 2017	After Sep.15, 2017	Amount
IEEE or IET member*	<input type="checkbox"/> 3500 CNY	<input type="checkbox"/> 3800 CNY	
Non-member	<input type="checkbox"/> 3800 CNY	<input type="checkbox"/> 4100 CNY	
Student	<input type="checkbox"/> 2400 CNY	<input type="checkbox"/> 2700 CNY	
Extra banquet ticket	<input type="checkbox"/> 300 CNY		
Extra pages	<input type="checkbox"/> 400 CNY / page		
Tutorial	<input type="checkbox"/> T-1&T-2&T-3&T-4 RMB 200		
<input type="checkbox"/> Vegetarian	<input type="checkbox"/> Need hardcopy Proceedings 500 CNY <input type="checkbox"/> Don't need hardcopy Proceedings		
Total Amount			CNY

(*IEEE or IETMember)* Member Number: _____

The registration fee covers:

- Admission to all the sessions;
- Three days' meals (Oct.25-28,2017) including the reception (Evening of Oct.26) and the banquet (Evening of Oct.28); Coffee Breaks;
- A conference kit (with a conference bag, a program brochure, and a USB with E-Proceedings).

(The tutorial fee covers the lunch on Oct.25 and tutorial materials. Please visit the conference website for details of the tutorials.)

3. Payment Methods

1) <input type="checkbox"/> Credit Card Date of Payment _____	<u>Please Click Here for Credit Card Payment</u>	_____ CNY
2) <input type="checkbox"/> Bank Transfer Remit date _____ Note: If it is not possible for you to transfer CNY, please transfer USD based on the USD/CNY exchange rate of the day of transfer.	Sender's Name _____ Account Name: <u>GUILIN COMFORT INTERNATIONAL TRAVEL SERVICE CO.,LTD.</u> Account Number: <u>6000420109025988</u> Bank Name: <u>GUILIN BANK CO., LTD</u> Bank address: <u>NO.76 ZHONGSHAN SOUTH ROAD, GUILIN,CHINA</u> Swift Code: <u>GLBKCNBG</u> Attn: <u>ASICON 2017</u>	_____ CNY

3) <input type="checkbox"/> Bank Draft/Check Remit date _____	I have enclosed herewith a bank draft/check made payable to Fudan University and sent to Jiating Sheng	_____ CNY
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Please send the Registration Form and Payment Receipt to Jiating Sheng by Email or Fax

Email: jtsheng@fudan.edu.cn

Fax: +86-21-65648267

Mailing address: School of Microelectronics, Fudan University,
220 Handan Road, Shanghai, 200433, China

● Registration Desk

The conference registration desk will be located at Guiyang Pullman Hotel. The conference registration will be open on Oct. 25 (8: 00~20: 00), Oct. 26~Oct. 28 (8: 00~17: 45). And the registration desk will keep available at the same site throughout the whole conference.

● Transportation

How to get to Guiyang:

- By Air:
 - (1) From Hong Kong to Guiyang (2 hours): There are about 1 flights daily, supplied by Hong Kong Air Lines.
 - (2) From Beijing to Guiyang (3 hours): There are dozens of flights daily, supplied by China Airline, China Eastern Airline, China Southern Airline and so on .
 - (3) From Shanghai to Guiyang (3 hours): There are more than 10 flights daily, supplied by China Eastern Airline, China Southern Airline, Shanghai Airline and so on.
 - (4) From Guangzhou to Guiyang(1.5 hours): There are more than 10 flights daily, supplied by China Eastern Airline, China Southern Airline.
- By Train:
 - (1) From Guangzhou South Railway Station to Guiyang North Railway Station (5-6 hours by bullet train): There are more than 20 bullet trains daily and so on.
 - (2) From Kunming South Railway Station to Guiyang North Railway Station (2-2.5 hours by bullet train): There are dozens of trains daily and so on.

How to get to the Pullman Guiyang:

- From Airport:

It takes about 15 minutes from Guiyang Longdongbao International Airport to Hotel by car. Taxi is recommended.
- From Railway Station:
 - (1) Guiyang Railway Station: Taxi takes about 5 minutes to hotel;
 - (2) Guiyang North Railway Station: Taxi takes about 40 minutes to hotel

● Weather

The average temperature during conference time in Guiyang is around 11°C~19°C.

● Visa

All the foreign travelers to China must have a valid visa. Visas may be obtained from the Chinese Embassy or Consulate in most major cities around the world. A conference attendee will be mailed an official invitation letter for visa application after he or she fills and returns the Visa Application Form (<http://www.asicon.org>) to asicon_org@fudan.edu.cn timely.

● Awards

Excellent Student Paper Awards will be announced at the banquet on Oct. 28. To be qualified for the Excellent Student Paper Award, the paper must be presented by the student himself or herself (1st author). The Technical Program Committee and Organizing Committee will choose through public appraisal some excellent student papers from the candidates.

Paper Presentation Information

The ASICON 2017 will have oral and poster sessions. All the papers included in the conference program should be presented in English by one of the authors at the arranged sessions.

● Oral Presentation

Presentation time:

Invited paper (20~30 minutes): 15~25 min talk + 5 min Q/A

Regular paper (12~15 minutes): 10~12 min talk + 2~3 min Q/A

Computer and digital projector will be provided in each meeting room.

● Poster Presentation

Poster size: 120 cm (high) × 100 cm (wide)

Poster Session 1:

Setup time: 8: 30-17: 30 on Oct. 26

Presentation time: 17: 45-18: 45 on Oct. 26 (on the spot)

Display time: 8: 30-21: 00 on Oct. 26

Poster Session 2:

Setup time: 8: 30-17: 30 on Oct. 27

Presentation time: 17: 45-18: 45 on Oct. 27 (on the spot)

Display time: 8: 30-21: 00 on Oct. 27

Thumb pins, adhesive tapes, and scissors will be provided at the registration desk. The poster should be taken off by 21: 30 by the author if he or she would like to keep it. After that time, it will be removed and be regarded as being discarded by the authors.

● Coffee Break

Complementary coffee/tea will be served in each morning/afternoon session. The break will take place in general at 10: 00-10: 15 during morning sessions and 15: 30-15: 45 during afternoon sessions. Due to time schedule of different sessions, the actual break time may have slight variation. Coffee/tea will be served in about half-hour duration.

● Meeting Room Location

Meeting Room	Location
Grand Ball Room	3 rd Floor, Pullman Hotel
Sapphire Room	3 rd Floor, Pullman Hotel
Jade Room 1	3 rd Floor, Pullman Hotel
Jade Room 2	3 rd Floor, Pullman Hotel
Jade Room 3	3 rd Floor, Pullman Hotel

ASICON 2017 Technical Program Overview

Date	Time	Sapphire Room	Jade Room 1	Jade Room 2	Jade Room 3
Oct.25	AM 9:00	Tutorial Session T-1 & T-2			
	PM 2:00	Tutorial Session T-3 & T-4			
Oct.26	8:30-10:30	Opening & Keynote Speech K1-1 & K1-2 (Grand Ball Room)			
	11:00-11:45	Keynote Speech K1-3 (Ballroom)			
	13:30-15:30	Session A1 Memory (1)	Session B1 High Resolution Data Converter	Session C1 Low Power Digital Techniques (1)	Session D1 CAD (1)
	15:45-17:45	Session A2: RF Design Techniques (1)	Session B2 Analog Techniques (1)	Session C2 Energy-Efficient Information Processing	Session D2 New Device & Advanced Techniques (1)
	17:45-18:45	Poster Session 1			
	19:00-21:00	Reception			
Oct.27..	8:30-10:00	Keynote Speech K2-1 & K2-2 (Grand Ball Room)			
	10:15-12:15	Session A3 Memory (2)	Session B3 Efficient Circuits for Biomedical Systems	Session C3 Low Power Digital Techniques (2)	Session D3 CAD (2)
	13:30-15:30	Session A4 Special Session: Biomedical Circuits and System	Session B4 Analog Techniques (2)	Session C4 Low Power Digital Techniques (3)	Session D4 New Device & Advanced Techniques (2)
	15:45-17:45	Session A5 Special Session: Sensory Circuits and Systems	Session B5 High Speed Data Converter	Session C5 VLSI for Emerging Applications	Session D5 Reliability in New Devices
	17:45-18:45	Poster Session 2			
Oct.28	8:30-10:00	Keynote Speech K3-1 & K3-2 (Grand Ball Room)			
	10:15-12:15	Session A6 Special Session: Low Power Digital Techniques	Session B6 Power Conversion and Management	Session C6 Low Power SoCs	Session D6 CAD (3)
	13:30-15:30	Session A7 Sensors and Display	Session B7 RF Design Techniques (2)	Session C7 Special Session Neural Network: Efficient Implementations and Applications	Session D7 New Device & Advanced Techniques (3)
	15:45-17:45	Session A8 Low Power VLSI for Communication	Session B8 RF Design Techniques (3)	Session C8 Circuits and Systems for IoT	Session D8 New Device & Advanced Techniques (4)
	19:00-21:00	Closing & Banquet			

Tutorial Session

Wednesday, October 25, 9:00 – 17:15
3rd Floor Hotel Pullman, Guiyang

Tutorial Session T-1 & T-2

9:00-10:30 T-1 Electrostatic discharge protection of consumer electronics: challenges and solutions

Oct. 25 **(Tutorial)** Prof. J.J.Liou

Sapphire Room University of Central Florida, USA

10:45-12:15 T-2 Circuit Simulation Technique: From Device Data to Circuit Performance

Oct. 25 **(Tutorial)** Prof. Mansun Chan

Sapphire Room Hong Kong University of Science & Technology, HK

Tutorial Session T-3 & T-4

14:00-15:30 T-3 Protecting cryptographic integrated circuits with side-channel information

Oct. 25 **(Tutorial)** Prof. Makoto Nagata

Sapphire Room Kobe University, Japan

15:45-17:15 T-4 Smart Image Sensors and applications to 3D range-finding

Oct. 25 **(Tutorial)** Prof. Makoto Ikeda

Sapphire Room University of Tokyo, Japan

Technical Session

Thursday, Oct. 26

Opening & Keynote Speech K1-1 & K1-2

8:30-9:00

Oct. 26

GrandBall Room

Opening Ceremony

9:00-9:45 K1-1

Oct. 26 (Keynote)

GrandBall Room

Data Converters for mobile and autonomous applications

Prof. Franco Maloberti, President of IEEE CASS

University of Pavia, Italy

9:45-10:30 K1-2

Oct. 26 (Keynote)

GrandBall Room

Evolution and Revolution in Devices and Systems

Dr. MeiKeiIeong, CTO of ASTRI

ASTRI, HK

Coffee Break

Keynote Speech K1-3

11:00-11:45 K1-3

Oct. 26 (Keynote)

GrandBall Room

Systems to Silicon: Faster and Smarter

Dr. Miao Liu, President of digital IC automatic design group

Cadence, USA

Coffee Break

SA1 Memory (1)

Session Chair: Toshiro Hiramoto, The University of Tokyo, Japan

13:30 SA1-1

Oct. 26 (Invited)

Sapphire Room

High Speed Negative Capacitance Ferroelectric Memory

Chun-Yen Chang, Chia-Chi Fan, Chien Liu, Yu-Chien Chiu, Chun-Hu Cheng

National Chiao Tung University, Taiwan

14:00 SA1-2

Oct. 26 (Invited)

Sapphire Room

Development Trends of Embedded NVM Technology

TianShen Tang, Hao Ni, Zijian Zhao, Yao Zhou

Semiconductor Manufacturing International Corporation, China

14:30 SA1-3

Oct. 26 (Invited)

Sapphire Room

1T2R: A Novel Memory Cell Design to Resolve Single-Event Upset in RRAM Arrays

Amr M.S.Tosson, Shimeng Yu, Mohab H. Anis, Lan Wei

University of Waterloo, Canada

15:00 SA1-4

Oct. 26

Sapphire Room

ReRAM Write Circuit with Dynamic Uniform and Small Overshoot Compliance Current under PVT Variations

Yun Yin, Junlin Gou, Junyi Wang, Yarong Fu, Xiaoyong Xue, Yinyin Lin

Fudan University, China

15:15 SA1-5

Oct. 26

Sapphire Room

An efficient parity rearrangement coding scheme for RRAM thermal crosstalk effects

Yun Li, Haihua Shen, Ce Li, Feng Zhang

Institute of Microelectronics of Chinese Academy of Sciences, China

SB1 High Resolution Data Converter

Session Chair: Weitao Li, Research Institute of Tsinghua University in Shenzhen, China

- 13:30 SB1-1** **SAR+DS ADC with Open-Loop Integrator using Dynamic Amplifier**
Oct. 26 **(Invited)** Akira Matsuzawa, Masaya Miyahara
Jade Room 1 Tokyo Institute of Technology, Japan
- 14:00 SB1-2** **A 0.87 mW 7MHz-BW 76dB-SNDR Passive Noise-Shaping Modulator Based On A SAR ADC**
Oct. 26 Zhiyuan Dai, Hang Hu, Manxin Li, Fan Ye, Junyan Ren
Jade Room 1 Fudan University, China
- 14:15 SB1-3** **A 13-bit Non-binary Weighted SAR ADC with Bridge Structure Using Digital Calibration for Capacitor Weight Error**
Oct. 26 Xiaoqing Chen, Fan Ye, Junyan Ren
Jade Room 1 Fudan University, China
- 14:30 SB1-4** **Auxiliary Testability Design Schemes for CMOS DACs with Ultrahigh Sampling Rates**
Oct. 26 Bao Li, Long Zhao, Yuhua Cheng
Jade Room 1 Peking University, China
- 14:45 SB1-5** **A 101 dB SNDR 3.7mW Switched-Capacitor $\Sigma\Delta$ ADC using tri-level quantization**
Oct. 26 Yumei Ma, Mengfei Ji, Yuping Guo, Yuchun Chang
Jade Room 1 Jilin University, China
- 15:00 SB1-6** **A highly linear voltage-to-time converter with variable conversion gain for time-based ADCs**
Oct. 26 Yan Ye, Weili Han, Haiyue Yan, Fujiang Lin
Jade Room 1 Uniuniversity of science and technology of China, China
- 15:15 SB1-7** **An On-Chip Signal Conditioning Delta-Sigma ADC for Micro-Mechanical Gyroscope Applications**
Oct. 26 Yongsheng Wang, Yang Liu, Xunzhi Zhou, Anyi Wang, Bei Cao, Fengchang Lai
Jade Room 1 Harbin Institute of Technology, China

SC1 Low-Power Digital Techniques (1)

Session Chair: Jun Han, Fudan University, China

- 13:30 SC1-1** **Soft Error Tolerant Latch Designs with Low Power Consumption**
Oct. 26 **(Invited)** Saki Tajima, Nozomu Togawa, Masao Yanagisawa, Youhua Shi
Jade Room 2 Waseda University, Japan
- 14:00 SC1-2** **How Close to the CMOS Voltage Scaling Limit for FinFET Technology? -- Near-Threshold Computing and Stochastic Computing**
Oct. 26 **(Invited)** Runsheng Wang, Xiaobo Jiang, Shaofeng Guo, Ru Huang
Jade Room 2 Peking University, China
- 14:30 SC1-3** **A Highly Reliable Lightweight PUF Circuit with Temperature and Voltage Compensated for Secure Chip Identification**
Oct. 26 Li Gang, Wang Pengjun, Zhang Yuejun
Jade Room 2 Ningbo University, China
- 14:45 SC1-4** **Floorplan-Driven High-Level Synthesis using Volatile/Non-volatile Registers for Hybrid Energy-Harvesting Systems**
Oct. 26 Daiki Asai, Masao Yanagisawa, Nozomu Togawa
Jade Room 2 Waseda University, Japan
- 15:00 SC1-5** **An All-N-Type Dynamic Adder for Ultra-Low-Leakage IoT Devices**
Oct. 26 Ya-Bei Fang, Pei-Yuan Chou, Bo-Hao Chen, Tay-Jyi Lin, Jinn-Shyan Wang
Jade Room 2 National Chung-Cheng University, Taiwan
- 15:15 SC1-6** **A New Error Masking Flip-flop With One Cycle Correction Penalty**

Oct. 26 Zhenqiang Yong, Xiaoyan Xiang, Chen Chen, Jianyi Meng
Jade Room 2 Fudan University, China

SD1 CAD (1)

Session Chair:	Mansun Chan, HKUST, HK
13:30 SD1-1	Fast Two-Dimensional Finite Element Analysis for Power Network DC Integrity Checks of PCBs
Oct. 26 (Invited) Jade Room 3	Wei He, Hengyang Zhao, Zhongdong Qi, Hai-Bao Chen, Sheldon X.D. Tan Shanghai Jiao Tong University, China
14:00 SD1-2	Overview of High-Efficiency Ant Colony Optimization (ACO)-based Adaptive Routings for Traffic Balancing in Network-on-Chip Systems
Oct. 26 (Invited) Jade Room 3	En-Jui Chang, An-Yeu (Andy) Wu National Taiwan University, Taiwan
14:30 SD1-3	Cut Redistribution and DSA Templates Assignment for Unidirectional Design
Oct. 26 Jade Room 3	Ye Huang, Xingquan Li, Wenxing Zhu, Jianli Chen Fuzhou University, China
14:45 SD1-4	A Novel Layout Automation Flow to Facilitate Test Chip Design for Standard Cell Characterization
Oct. 26 Jade Room 3	Ludan Yang, Weiwei Pan, Zheng Shi, Yongjun Zheng Zhejiang University, China
15:00 SD1-5	Dynamic Temperature-Aware Reliability Modeling for Multi-Branch Interconnect Trees
Oct. 26 Jade Room 3	Jiangtao Peng, Hai-Bao Chen, Hengyang Zhaoy, Zeyu Suny, Sheldon X.-D. Tany Shanghai Jiao Tong University, China
15:15 SD1-6	ILP-based Fault-Tolerant Topology Synthesis for Application-Specific Network-on-Chip
Oct. 26 Jade Room 3	Zhigang Li, Jinglei Huang, Qi Xu, Song Chen University of Science and Technology of China, China

Coffee Break

SA2 RF Design Techniques (1)

Session Chair:	Francois RIVET, University of Bordeaux, France
15:45 SA2-1	Wideband Power Amplifier Predistortion : Trends, Challenges and Solutions
Oct. 26 (Invited) Sapphire Room	Patricia Desgresys, Venkata Narasimha Manyam, Kelly Tchambake, Dang-Kien Germain Pham, Chadi Jabbour LTCl, Telecom ParisTech, Universite Paris-Saclay, France
16:15 SA2-2	An Wide Locking Range Injection-Locked Frequency Divider by Dual Resonance Tank
Oct. 26 Sapphire Room	Wen-Cheng Lai, Sheng-Lyang Jang, and Shih-Jie Jian National Taiwan University of Science and Technology, Taiwan
16:30 SA2-3	Design of 258GHz Second Order Harmonic Injection Locked VCO
Oct. 26 Sapphire Room	Yong Xu, Fei Zhao, Yuanliang Wu University of Army Engineering, China
16:45 SA2-4	A LTE Digital Mixer with 25% Duty Quadrature 4-phase clocks
Oct. 26 Sapphire Room	Haijun Shao, Dan Fang, Pan Xue, Hongguang Zhang, Yilei Shen, Yumei Huang, Gan Guo, Zhiliang Hong Fudan University, China
17:00 SA2-5	A CMOS Transceiver RFIC for China Geo-Radio Standard
Oct. 26 Sapphire Room	Zhao Wang, Dihu Chen, Jianping Guo Sun Yat-sen University, China

SB2 Analog Techniques (1)

	Session Chair:	Yuhua Cheng, Peking University, China
15:45	SB2-1	Design Trends in Smart Gate Driver ICs for Power MOSFETs and IGBTs
Oct. 26	(Invited)	J. Chen, W. T. Ng
	Jade Room 1	University of Toronto, Canada
16:15	SB2-2	Characterization of Impacts of Parasitics on the Performance of High-Speed Analog Circuits
Oct. 26	(Invited)	Long Zhao, Josh Yang, Tianshen Tang, Yuhua Cheng
	Jade Room 1	Peking University, China
16:45	SB2-3	A 0.18μm High-voltage Area Efficient Integrated Gate Driver for Piston Engine Fuel Injection Control SoC
Oct. 26		Qinmiao Kang, Ming Zhou
	Jade Room 1	Tsinghua University, China
17:00	SB2-4	An Output-capacitor-less Low-dropout Regulator with Transient-improved Technique
Oct. 26		Xin Liu, Yu Liu, Yanbin Xiao, Xiaohua Fan, Haiying Zhang
	Jade Room 1	Institute of Microelectronics of Chinese Academy of Sciences, China
17:15	SB2-5	A High-Efficiency Class E Power Amplifier with Integrated Finite DC Feed Inductance
Oct. 26		Haobo Ruan, Tingyuan Yan, Yumei Huang
	Jade Room 1	Fudan University, China
17:30	SB2-6	A Low-Offset Dynamic Comparator with Input Offset-Cancellation
Oct. 26		Ruihan Pei, Jia Liu, Xian Tang, Fule Li, Zhihua Wang
	Jade Room 1	Tsinghua University, China

SC2 Energy-Efficient Information Processing

	Session Chair:	David Pan, University of Texas at Austin, USA
15:45	SC2-1	Cooptimization of Emerging Devices and Architectures for Energy-Efficient Computing
Oct. 26	(Invited)	An Chen
	Jade Room 2	SRC / IBM, USA
16:15	SC2-2	Challenges of Emerging Memory and Memristor Based Circuits: Nonvolatile Logics, IoT Security, Deep Learning and Neuromorphic Computing
Oct. 26	(Invited)	Chunmeng Dou, Wei-Hao Chen, Yi-Ju Chen, Huan-Ting Lin, Wei-Yu Lin, Mon-Shu Ho, Meng-Fan Chang
	Jade Room 2	National Tsinghua University, Taiwan
16:45	SC2-3	Memristors for Emerging Memory and Computing Applications
Oct. 26	(Invited)	Qingxi Duan, Teng Zhang, Minghui Yin, Caidie Cheng, Liying Xu, Yuchao Yang, Ru Huang
	Jade Room 2	Peking University, China
17:15	SC2-4	A Low Bit-width Parameters Representation Method for Hardware-oriented Convolution Neural Networks
Oct. 26		Qiang Chen, Chen Xin, Chenglong Zou, Xinan Wang, Bo Wang
	Jade Room 2	Peking University, China
17:30	SC2-5	High-Speed FPGA Implementation of Orthogonal Matching Pursuit for Analog to Information Converter
Oct. 26		SuJuan Liu, Ning Lv, Zisheng Wang
	Jade Room 2	Beijing University of Technology, China

SD2 New Devices and Advanced Tehnologies (1)

Session Chair:	Rui Zhang, Zhejiang University, China	
15:45	SD2-1	Looking back and forward: the execution dilemma and the importance of innovation in the semiconductor industry
Oct. 26	(Invited)	Domenico Rossi ST Microelectronics, Italy
Jade Room 3		
16:15	SD2-2	Research Advances and Applications of 3D Integration
Oct. 26	(Invited)	Kuan-Neng Chen NCTU, Taiwan
Jade Room 3		
16:45	SD2-3	Nonvolatile Memory with 2D Materials for Floating Storage
Oct. 26	(Invited)	ChaoSung Lai Chang Guang University, Taiwan
Jade Room 3		
17:15	SD2-4	Development and Characterization of TaN Thin Film Resistor with CMOS Compatible Fabrication Process
Oct. 26		Xiaoxu Kang, Limin Zhu, Xingwang Zhu, Qingyun Zuo, Xiaolan Zhong, Shoumian Chen, Yuhang Zhao, Shanshan Liu, Hanwei Lu, Jianmin Wang, Wei Wang, Bo Zhang Shanghai ICR&D Center, China
Jade Room 3		
17:30	SD2-5	Vertical Power Diodes based on Bulk GaN Substrates
Oct. 26		Liang Zheng, Lin-Jie Yu, Lin Chen, Qing-Qing Sun, Wei Huang, Hao Zhu, David Wei Zhang Fudan University, China
Jade Room 3		
17:45	SD2-6	Advanced Interconnection Technology, High K/Metal gate technology and other VLSI New Processing, New Technologies
Oct. 26	(Invited)	Tao Chu Zhejiang University, China
Jade Room 3		

Oct. 26 17:45-18:45

Poster Session I

P1-01	High Speed Vedic Multiplier Used Vedic Mathematics
Oct. 26	Dravik Kishor, Bhai Kahar Parul University, India
P1-02	A Harmonic-Free Cell-Based All-Digital Delay-Locked Loop for Die-to-Die Clock Synchronization of 3-D IC
Oct. 26	Tailong Xu, Feng Xue, Zhikuang Cai, Xinning Liu, Shuo Meng Hefei University, China
P1-03	76μW, 58-dB SNDR Analog Front-End Chip For Implantable Intraocular Pressure Detection
Oct. 26	Chengying Chen, Liming Chen, Xinghua Wang, Feng Zhang Xiamen University of Technology, China
P1-04	A VCO with Dynamic Body Injection and Class-C Technique
Oct. 26	Wen-Cheng Lai, Sheng-Lyang Jang, Bi-Shen Shih National Taiwan University of Science and Technology, Taiwan
P1-05	Design of a voltage-tunable pre-emphasis circuit utilizing a pseudo-differential cascode architecture
Oct. 26	Wenhui Li, Yawei Zhang, Weiwei Chen

- Ningbo University, China
- P1-06** **A 320MS/s 7-b Flash-SAR ADC with Preamplifier Sharing Technique**
 Oct. 26 Hang Hu, Zhiyuan Dai, Manxin Li, Fan Ye, Junyan Ren
 Fudan University, China
- P1-07** **A Gain Factor Controlled SUMPLE Algorithm and System**
 Oct. 26 Leiou Wang, Donghui Wang
 Chinese Academy of Sciences, China
- P1-08** **A 1.0-7.0 GHz Inductorless RF Mixer with Multiple Feedback and Active Load in 40-nm CMOS**
 Oct. 26 Xu Yan, Lu Yang, Hao Zhang, Jili Zhang, Fujiang Lin
 University of Science and Technology of China, China
- P1-09** **Research of A Reconfigurable Coarse-grained Cryptographic Processing Unit based on Different Operation Similar Structure**
 Oct. 26 Longmei Nan, Xiaoyang Zeng, Zhouchuang Wang, Yiran Du, Wei Li
 Fudan University, China
- P1-10** **A Novel Vertical Semi-Floating Gate Transistor for High-Density Ultrafast Memory**
 Oct. 26 Zheng-Yuan Su, Jun Wu, Yao Yao, Zhi-Yuan Ye, Peng-Fei Wang
 Fudan University, China
- P1-11** **A Novel Programmable Pulse-Broadening Time Amplifier Controlled by Node Capacitance**
 Oct. 26 Jiangtao Gu, Bo Wang, Chao Zhang, Tingbing Ouyang, Lizhao Gao
 Peking University, China
- P1-12** **Atomic Layer Deposited Hf_{0.5}Zr_{0.5}O₂-based Flexible RRAM**
 Oct. 26 Tian-Yu Wang, Lin-Jie Yu, Lin chen, Hao Liu, Hao Zhu, Qing-Qing Sun, Shi-Jin Ding, Peng Zhou, David Wei Zhang
 Fudan University, China
- P1-13** **Design of a Novel Ternary SRAM Sense Amplifier Using CNFET**
 Oct. 26 Zizhao Liu, Tao Pan, Song Jia, Yuan Wang
 Peking University, China
- P1-14** **A Neural Network Circuit with Associative Learning and Forgetting Process Based on Memristor Neuromorphic Device**
 Oct. 26 Xiaoqiang Lv, Yimao Cai, Yuchao Yang, Zhizhen Yu, Yichen Fang, Zongwei Wang, Lindong Wu, Jianfeng Liu, Wanrong Zhang, Ru Huang
 Peking University, China
- P1-15** **A 40V Monolithic Ultrasonic Motor Driver**
 Oct. 26 Ping Luo, Kangle Wang, Shuangjie Qiu, Zelang Liu, Long Huang
 University of Electronic Science & Technology of China, China
- P1-16** **Roles of the Gate Length and Width of the Transistors in Increasing the Single Event Upset Resistance of SRAM cells**
 Oct. 26 Zhongshan Zheng, Zhentao Li, Gengsheng Chen, Jiajun Luo, Zhengsheng Han
 Institute of Microelectronics of Chinese Academy of Sciences, China
- P1-17** **Low-Cost Resilient Radiation Hardened Flip-Flop Design**
 Oct. 26 Liyi Xiao, Chunhua Qi, Tianqi Wang, Hongchen Li, Jiaqiang Li
 Harbin Institute of Technology, China
- P1-18** **Heterogeneous Computing for CNN**
 Oct. 26 Huizi Zhang, Chang Wu, Xiao Hu
 Fudan University, China
- P1-19** **Optimization of Operational Amplifier Settling Time by Adjusting Secondary Poles Based on gm/ID Design**

- Oct. 26 Jun Qiao, Xiao Wang, Yaohong Zhao
Chinese Academy of Sciences, China
- P1-20 Residual stress study of thin films deposited by atomic layer deposition**
- Oct. 26 Zhen Zhu, Emma Salmi, Sauli Virtanen
Beneq Oy, Finland
- P1-21 A Fully Pipelined Hardware Architecture for Convolutional Neural Network with Low Memory Usage and DRAM Bandwidth**
- Oct. 26 Zhiwei Li, Yan Li, Song Chen, Feng Wu
University of Science and Technology of China, China
- P1-22 A Radiation Hardened Low-Noise Voltage-Controlled-Oscillator using Negative Feedback based Multipath- Current-Releasing Technology**
- Oct. 26 Hengzhou Yuan, Jianjun Chen, Bin Liang, Yang Guo
National University of Defense Technology, China
- P1-23 A Stacked-packaged 16-channel ADC for Ultrasound Application**
- Oct. 26 Yimin Wu, Junyan Ren, Fan Ye, Yongzhen Chen
Fudan University, China
- P1-24 Analytical Models for Channel Potential and Drain Current in AlGaIn/GaN HEMT Devices**
- Oct. 26 Haisheng Qian, GUANGXI HU, Laigui Hu, Xing Zhou, Ran Liu, and Lirong Zheng
Fudan University, China
- P1-25 An efficient HMAC processor based on the SHA-3 HASH function**
- Oct. 26 Junhui Li, Liji Wu, Xiangmin Zhang
Tsinghua University, China
- P1-26 An improved Equivalent Circuit Model for Antenna: Modeling and Parameter Extraction**
- Oct. 26 Hansheng Wang, Minghui Zhang, Weiliang He, Lu Tang, Bin Jiang
Southeast University, China
- P1-27 Parallel Sparse LU Decomposition Using FPGA with an Efficient Cache Architecture**
- Oct. 26 Xiang Ge, Hengliang Zhu, Fan Yang, Lingli Wang, Xuan Zeng
Fudan University, China
- P1-28 Study of 64-bit Booth Asynchronous Multiplier based on FPGA**
- Oct. 26 Xiaoqing Liu, Anping He, Caihong Li, Guangbo Feng, Zhang Jilin
Lanzhou University, China
- P1-29 A 20MHz CTIA ROIC for InGaAs Focal Plane Array**
- Oct. 26 Liang Li, Ruizhi Sun, Ruoxi Wang, Fanjun Zang, Tao Jiang, Yang Li, Xinyang Wang, Yuchun Chang
Jilin University, China
- P1-30 Memristor-Based IMPLY Logic Design for Full Adders**
- Oct. 26 Mengting Li, Wenhao Sun, Song Chen, Feng Wu
University of Science and Technology of China, China
- P1-31 A Synchronous Charge Extraction piezoelectric energy harvesting Circuit Based on precision active control peak detection with supplement energy**
- Oct. 26 Xiudeng Wang, Yinshui Xia, Xiaojing Zha, Yonggeng Tu, Ge Shi, Yidie Ye
Ningbo University, China
- P1-32 Implementation and optimization of A5-1 algorithm on Coarse-Grained Reconfigurable Cryptographic Logic Array**
- Oct. 26 Liu Min, Li Wei, Yan YingJian
Zhengzhou Institute of Information Science and Technology, China
- P1-33 Improving DFA on AES using all-fault ciphertxts**

- Oct. 26 Yewen Ni, Xiaoxin Cui, Tian Wang, Yuanning Fan, Qiankun Han, Kefei Liu, Xiaole Cui
Peking University, China
P1-34 Application Space Exploration of a Multi-Fabric Reconfigurable System
- Oct. 26 Fan Feng, Li Li, Kun Wang, Feng Han, Hongbing Pan, Wei Li
Nanjing University, China
P1-35 A Noise-Shaping SAR ADC with Dual Error-Feedback Paths and Alternate DACs
- Oct. 26 Jiaqi Yang, Jili Zhang, Xuefei Bai, Fujiang Lin
University of Science and Technology of China, China
P1-36 A Background Time-skew Calibration Technique in Flash-Assisted Time-Interleaved SAR ADCs
- Oct. 26 Yongzhen Chen, Yimin Wu, Fubiao Cao, Fan Ye, Junyan Ren
Fudan University, China
P1-37 Influence of heat source size on Thermal resistance of AlGaIn/GaN HEMT
- Oct. 26 Chunsheng Guo, Ju Meng, Zhiheng Liao, Shiwei Feng, Xun Wang, Lin Luo
Beijing University of Technology, China
P1-38 An Optimized Topology Reconfiguration Bidirectional Searching Fault-tolerant Algorithm for REMesh Network-on-Chip
- Oct. 26 Fang Fa Fu, Na Niu, Xiaohu Xian, Jinxiang Wang, Fengchang Lai
Harbin Institute of Technology, China
P1-39 A 1.0-to-2.4GHz Wideband VCO with Uniform Sub-band Interval and Constant Tuning Gain
- Oct. 26 Chenyang Kong, Xiaodong Liu, Weigang Xu, Zhangwen Tang
Fudan University, China
P1-40 A Low Cost and High Speed CSD-based Symmetric Transpose Block FIR Implementation
- Oct. 26 Jinghao Ye, Youhua Shi, Nozomu Togawa, Masao Yanagisawa
Waseda University, Japan
P1-41 FPGA-based Efficient Implementation of SURF Algorithm
- Oct. 26 Ying Zhang, Yujie Huang, Jun Han, Xiaoyang Zeng
Fudan University, China
P1-42 A Configurable Nonlinear Operation Unit For Neural Network Accelerator
- Oct. 26 Yujie Cai, Xin Li, Jun Han, Xiaoyang Zeng
Fudan University, China
P1-43 A Deep Research on the Chip Verification Platform Based on Network
- Oct. 26 Chuanliang Kang, Pei Yang, Jian Wang, Jinmai Lai
Fudan University, China
P1-45 A New Countermeasure against Side Channel Attack for HMAC-SM3 Hardware
- Oct. 26 Jiawei Ma, Xuguang Guan, Tong Zhou, Tao Sun
State Key Laboratory of Cryptology, China
P1-46 A Fully-Pipelined Hash Table Achieving Low-Latency And High Throughput Key-Value Retrieving System
- Oct. 26 Li Ding, Wenbo Yin
Fudan University, China
P1-47 A Low Input Power Charge Pump for Passive UHF RFID Applications
- Oct. 26 Dongsheng Liu, Jiao Wang, Xiangcheng Sun, Jin Yan, Hui Lin
Huazhong University of Science and Technology, China
P1-48 A State Recovery Design against Single-Event Transient in High-speed Phase

- Interpolation Clock and Data Recovery Circuit**
- Oct. 26 Jiawei Tan, Yang Guo, Jianjun Chen, Hengzhou Yuan, Xi Chen
National University of Defense Technology, China
- P1-50 Graphite Planar Resistive Switching Memory and its application in pattern recognition**
- Oct. 26 Lin-Jie Yu, Tian-Yu Wang, Lin Chen, Hao Zhu, Qing-Qing Sun, Shi-Jin Ding, Peng Zhou, David Wei Zhang
Fudan University, China
- P1-51 A method to speed up VLSI hierarchical physical design in floorplanning**
- Oct. 26 Yanling Zhou, Yunyao Yan, Wei Yan
Peking University, China
- P1-52 Power Optimization Based On Dual-Logic Using And-Xor-Inverter Graph**
- Oct. 26 Xuejiao Ma, Yinshui Xia
Ningbo University, China
- P1-53 PSR-Enhanced Low-Dropout Regulator Using Feedforward Supply Noise Rejection Technique**
- Oct. 26 Xin Ming, Xuan Zhang, Di Gao, Jia-hao Zhang, Bo Zhang
University of Electronic Science and Technology of China, China
- P1-54 A Fast and Accurate Fault Injection Platform for SRAM-Based FPGAs**
- Oct. 26 Rongsheng Zhang, Liyi Xiao, Jie Li
Harbin Institute of Technology, China
- P1-55 A Method to Estimate Cross-section of Circuits at RTL Levels**
- Oct. 26 Liyi Xiao, Anlong Li, Xuebing Cao, Hongchen Li, Rongsheng Zhang, Jie Li, Tianqi Wang
Harbin Institute of Technology, China
- P1-56 A Low Gain Error Two-Stage dB-Linear Variable Gain Amplifier in 0.35 μ m CMOS Process**
- Oct. 26 Wang Yongsheng, Li Xinzhi, Zhang Zhixin, Lai Fengchang
Harbin Institute of Technology, China
- P1-57 Low Frequency Noise Characteristics in p-Type MOSFET with Multilayer WSe₂ Channel and Al₂O₃ Back Gate Dielectric**
- Oct. 26 Hui Shen, Huiwen Yuan, Sitong Bu, Mingyue He, Daming Huang
Fudan University, China
- P1-58 Design of Ternary Pulsed Reversible Counter based on CNFET**
- Oct. 26 Kang Yaopeng, Wang Pengjun, Zhang Yuejun, Li Gang
Ningbo University, China
- P1-59 Delay and Area Optimization for FPRM Circuits Based on MSPSO Algorithm**
- Oct. 26 Mingbo Wang, Pengjun Wang, Qiang Fu, Huihong Zhang
Ningbo University, China
- P1-60 The Write Deduplication Mechanism Based on A Novel Low-Power Data Latched Sense Amplifier for A Magnetic Tunnel Junction Based Non-Volatile Memory**
- Oct. 26 Baofa Huang, Ningyuan Yin, Zhiyi Yu
Sun Yat-sen University, China
- P1-61 Implementation of an Energy-efficient Digital Baseband Controller Compatible with EPC Class-1 Gen-2 Standard**
- Oct. 26 Dongsheng Liu, Xiangcheng Sun, Jiao Wang, Fan Kang
Huazhong University of Science & Technology, China
- P1-62 LMS-FIR Based Digital Background Calibration for the Four-channel Time-Interleaved ADC**
- Oct. 26 Yongsheng Wang, Shanshan Li, Ruoyang Wang, Xiaowei Liu
Harbin Institute of Technology, China

- P1-63** **Optimization of the Amplifier's Input-Referred Noise for High Resolution Comparators**
 Oct. 26 Qichao He, Xiong Zhou, Qiang Li
 University of Electronic Science and Technology of China, China
- P1-64** **A Self-Powered Supply Circuit for Switching Mode Power Supply**
 Oct. 26 Yue Shi, Hongming Yu, Zekun Zhou
 Chengdu University of Information Technology, China
- P1-65** **Remote Embedded Simulation System for SW/HW Co-design Based On Dynamic Partial Reconfiguration**
 Oct. 26 Jiaqi Gu, Ruoyao Wang, Jian Wang, Jinmei Lai, Qinghua Duan
 Fudan University, China
- P1-66** **A 0.07-ppm/Step Differential Digitally Controlled Crystal Oscillator With Guaranteed Monotonicity**
 Oct. 26 Xiaodong Liu, Chenyang Kong, Yifan Gao, Zhangwen Tang
 Fudan University, China
- P1-67** **The configurable current flattening circuit for DPA countermeasures**
 Oct. 26 Yong Gu, Xu-guang Guan, Tong Zhou
 Beijing Academy of Information Science & Technology

Oct. 26 19:00-21:00

Reception

Technical Session

Friday, Oct. 27

Keynote Speech K2-1 & K2-2

- 8:30-9:15 K2-1 Nanocarbon Interconnects - from 1D to 3D**
Oct. 27 **(Keynote)** Prof. Cary Yang, Director, TENT Laboratory
GrandBall Room Santa Clara University, USA
- 9:15-10:00 K2-2 3D Heterogeneous Integration Enabling Next-Generation ICs**
Oct. 27 **(Keynote)** Prof. Albert Wang
GrandBall Room University of California, Riverside, USA

SA3 Memory (2)

Session Chair: Xiaoyong Xue, Fudan University, China

- 10:15 SA3-1 Parallel Nonvolatile Programming of Power-up States of SRAM Cells**
Oct. 27 **(Invited)** Toshiro Hiramoto, Tomoko Mizutani, Kiyoshi Takeuchi, Masaharu Kobayashi
Sapphire Room The University of Tokyo, Japan
- 10:45 SA3-2 Phase-Change Materials and Memory Devices for IoT Application**
Oct. 27 **(Invited)** You Yin
Sapphire Room Gunma University, Japan
- 11:15 SA3-3 A Two-Port SRAM Using a Single-Port Cell Array with a Self-Timed Write-after-Read Control Scheme to Save 47% Area & 63% Standby Power**
Oct. 27 Fujun Bai, Baoyu Xiong, Xiaofei Xue, Weizhe Song, Wu Baofeng, Ni Fu, Bing Yu, Huifu Duan, Xiaowei Han, Alessandro Minzoni, Qiwei Ren
Sapphire Room Xi'an Unic Semiconductors Co. Ltd, China
- 11:30 SA3-4 A 55nm Logic Process Compatible p-Flash Memory Array Fully Demonstrated with High Reliability**
Oct. 27 Jinghui Han, Yao Zhou, Hao Ni, Xiao Zheng, Yi Zhao
Sapphire Room Zhejiang University, China
- 11:45 SA3-5 Graphene Nanodots with High-K Dielectrics for Flash Memory Applications**
Oct. 27 Kai-Ping Chang, Han-Hsiang Tai, Jer-Chyi Wang, Chao-Sung Lai
Sapphire Room Chang Gung University, Taiwan

SB3 Efficient Circuits for Biomedical Systems

Session Chair: Te-Kuang Chiang, National University of Kaohsiung, Taiwan

- 10:15 SB3-1 The Next-Generation Brain Machine Interface System For Neuroscience Research and Neuroprosthetics Development**
Oct. 27 **(Invited)** Jan Van der Spiegel, Milin Zhang, Xilin Liu
Jade Room 1 University of Pennsylvania, USA
- 10:45 SB3-2 System Architecture of a Smart Binaural Hearing Aid Using a Mobile Computing Platform**
Oct. 27 **(Invited)** Yingdan Li, Fei Chen, Zhuoyi Sun, Zhaoyang Weng, Xian Tang, Hanjun Jiang, Zhihua Wang
Jade Room 1 Tsinghua University, China
- 11:15 SB3-3 An area efficient and low power EcoG front-end chip for digitalized subdural grid**

Oct. 27		Chenjie Dong, Han Jin, IkHwan Kim, Chenyu Wang, Yajie Qin, Lirong Zheng
Jade Room 1		Fudan University, China
11:30	SB3-4	A 20Mbps 5.8mw QPSK Transmitter Based on Injection Locking and Class-E PA for Wireless Biomedical Applications
Oct. 27		Yaxiong Lei, Xinpeng Xing, Haigang Feng, Zhihua Wang
Jade Room 1		Tsinghua University, China
11:45	SB3-5	A 0.5 V 60 nW Fully-Differential Log-Domain Band-Pass Filter with Tunable Cutoff Frequency for Biosensor Applications
Oct. 27		Jinyong Zhang, Shing-Chow Chan, Hui Li, Lei Wang
Jade Room 1		Shenzhen Institutes of Advanced Technology Chinese Academy of Science, China
12:00	SB3-6	A 110-dBΩ, 113-MHz Variable-Gain Transimpedance Amplifier for Flash 3D Imaging Systems
Oct. 27		Lei Yang, Shaowei Zhen, Jiongwei Zheng, Shuiqing Xi, Xinjiang Gao, Zengxin Liu, He Tang, Ping Luo, Bo Zhang
Jade Room 1		University of Electronic Science and Technology of China, China

SC3 Low-power Digital Techniques (2)

Session Chair: Xinggang Wang, Skyworks Solution, USA

10:15	SC3-1	An Outlier Detection Method and its Application to Multicore-Chip Power Estimation
Oct. 27	(Invited)	Yaguang Li, Pingqiang Zhou
Jade Room 2		ShanghaiTech University, China
10:45	SC3-2	Energy-efficient Standby-current Suppression with Bootstrapped Power-gating Technique
Oct. 27	(Invited)	Yingchieh Ho, Chen Hsu
Jade Room 2		National Dong Hwa University, Taiwan
11:15	SC3-3	Ultralow Power Loss Integratable High-voltage MOSFETs
Oct. 27	(Invited)	Xiaorong Luo, Weiwei Ge, Bo Zhang
Jade Room 2		University of Electronic Science and Technology of China, China
11:45	SC3-4	Optical Computing on Silicon-on-Insulator-Based Photonic Integrated Circuits
Oct. 27	(Invited)	Zheng Zhao, Zheng Wang, Zhoufeng Ying, Shounak Dhar, Ray T. Chen, and David Z. Pan
Jade Room 3		University of Texas at Austin, USA

SD3 CAD (2)

Session Chair: Jun Tao, Fudan University, China

10:15	SD3-1	A Universal Approach for Signal Dependent Circuit Reliability Simulation
Oct. 27	(Invited)	Lining Zhang, Chenyue Ma, Mansun Chan
Jade Room 3		HKUST, HK
10:45	SD3-2	Analysis of Sub-threshold Electron Transport Properties of Ultra-scaled Amorphous Phase Change Material Germanium Telluride
Oct. 27	(Invited)	Jie Liu, M.P. Anantram, Xu Xu, Jiwu Lu
Jade Room 3		University of Washington, USA
11:15	SD3-3	An On-line Debug Method for FPGAs
Oct. 27		Yipeng Yuan, Zhihua Feng, Xuegong Zhou
Jade Room 3		Fudan University, China
11:30	SD3-4	DTCO through Design Space Exploration by the Virtual FAB Range Pattern Matching Flow

Oct. 27		Liang Zhu, Yida Xie, Zhibo Ai
Jade Room 3		Synopsys, China
11:45	SD3-5	Design and Automatic Generation of Area-efficient Ring Oscillator Based Addressable Test Chips
Oct. 27		Xiaoxin Dou, Weiwei Pan, Zheng Shi, Yongjun Zheng
Jade Room 3		Zhejiang University, China
12:00	SD3-6	Synthesis and Optimization of Asynchronous Dual-rail Encoded Circuits based on Partial Acknowledgement
Oct. 27		Yu Zhou, Chun Shi, Zhengjie Deng, Alex Yakovlev
Jade Room 3		Hainan Normal University, China

Coffee Break

SA4 Special Session: Biomedical Circuits and Systems

	Session Chair:	Guoxing Wang, Shanghai Jiao Tong University, China
13:30	SA4-1	Design of a Closed-loop, Bi-directional Brain-Machine-Interface Integrated On-chip Spike Sorting
Oct. 27	(Invited)	Ting Ou, Deng Luo, Yuwei Zhang, Yiqiao Liao, Chang Cheng, Milin Zhang, Chun Zhang, Zihua Wang, Xiang Xie
Sapphire Room		Tsinghua University, China
14:00	SA4-2	A Fully Differential High Efficient ASK Demodulator for Biomedical Implantable Application
Oct. 27	(Invited)	Jie Zhou, Xi Chen, Tianzhun Wu, Guoxing Wang
Sapphire Room		Shanghai Jiao Tong University, China
14:30	SA4-3	Refractory Epilepsy: Localization, Detection, and Prediction
Oct. 27	(Invited)	E. Bou Assi, D. K. Nguyen, S. Rihana, M. Sawan
Sapphire Room		Polytechnique Montreal, Canada
15:00	SA4-4	Low Power FIR Filter Design for Wearable Devices Using Frequency Response Masking Technique
Oct. 27	(Invited)	Zhongxia Shang, Yang Zhao, Yong Lian
Sapphire Room		York University, Canada

SB4 Analog Techniques (2)

	Session Chair:	Akira Matsuzawa, Tokyo Institute of Technology, Japan
13:30	SB4-1	A New Short-Channel-Effect-Degraded Subthreshold Behavior Model for Elliptical Gate-All-Around MOSFET
Oct. 27	(Invited)	Te-Kuang Chiang, Ying-Wen Ko, Hong-Wun Gao, Yeong-Her Wang
Jade Room 1		EE of National University of Kaohsiung, Taiwan
14:00	SB4-2	High-Order Curvature-Compensated CMOS Bandgap Voltage Reference
Oct. 27		Qianneng Zhou, Feihong Cheng, Hongjuan Li, Kai Yan, Wei Luo
Jade Room 1		Chongqing University of Posts and Telecommunications
14:15	SB4-3	A 3.7ppm/°C Piece-Wise Compensated Bandgap Reference
Oct. 27		Quanwang Liu, Bo Zhang, Shaowei Zhen, Weidong Xue
Jade Room 1		UESTC, China
14:30	SB4-4	Low-Power and High-Frequency Ring Oscillator Design in 65nm CMOS Technology
Oct. 27		Chi-Hsien Yen, Mehdi Nasrollahpour, Sotoudeh Hamedi-Hagh
Jade Room 1		San Jose State University, USA
14:45	SB4-5	Design of 56 Gb/s PAM4 Wire-line Receiver With Ring VCO Based CDR in a

65 nm CMOS Technology

- Oct. 27
Jade Room 1
15:00 **SB4-6** **A New All-in-One Bandgap Reference and Robust Zero Temperature Coefficient (TC) point Current Reference Circuit**
Fangxu Lv, Jianye Wang, Dengjie Wang, Yongcong Liu, Ziqiang Wang
Air Force Engineering University, China
- Oct. 27
Jade Room 1
15:15 **SB4-7** **A 2.4GHz T/R Switch with ESD Protection for WLAN 802.11 b/g/n Applications**
Yan Chen, Xiaoling Tan, Bolin Yu, Chunxia Li, Yan Guo
Shenzhen Institute of Information Technology, China
- Oct. 27
Jade Room 1
15:45 **SB4-8** **A Novel Low-Power CMOS Bandpass Filter for WLAN Applications**
Jijian Shi, Tingting Mo
Shanghai Jiao Tong University, China

SC4 Low-power Digital Techniques (3)

Session Chair: Gerald E. Sobelman, University of Minnesota, USA

- 13:30** **SC4-1** **Fundamental Design Tradeoff and Performance Limitation of Electronic Circuits Based on Uncertainty Relationships**
Oct. 27 **(Invited)** Haruo Kobayashi, Isao Shimizu, Nobukazu Tsukiji, Miho Arai, Kazuyoshi Kubo, Hitoshi Aoki
Jade Room 2
Gunma University, Japan
- 14:00** **SC4-2** **Stochastic Computing Implementation of Trigonometric and Hyperbolic Functions**
Oct. 27 **(Invited)** Lian Huai, Peng Li, Gerald E. Sobelman, David J. Lilja
Jade Room 2
University of Minnesota, USA
- 14:30** **SC4-3** **A novel adaptive general current drive circuit**
Oct. 27 Yujie Chen, Ningmei Yu, Hejiu Zhang, Keren Li, Nan Lyu
Jade Room 2
Xi'an University of Technology, China
- 14:45** **SC4-4** **Fp2 Arithmetic Acceleration Based on Modified Barrett Modular Multiplication Algorithm**
Oct. 27 Yalong Pang, Ying Zhang, Jun Han, Xiaoyang Zeng
Jade Room 2
Fudan University, China
- 15:00** **SC4-5** **IZIP: In-Place Zero Overhead Interconnect Protection via PIP Redundancy**
Oct. 27 Yi Luo, Adrian Evans, Shi-Jie Wen, Rick Wong, Gengsheng Chen
Jade Room 2
Fudan University, China
- 15:15** **SC4-6** **An On-Chip Circuit for Timing Measurement of SRAM IP**
Oct. 27 Xianjie Long, Qin Wang, Jianfei Jiang, Nin Guan
Jade Room 2
Shanghai Jiao Tong University, China

SD4 New Devices and Advanced Tehnologies (2)

Session Chair: Jifa Hao, ON Semiconductor, USA

- 13:30** **SD4-1** **Interface Engineering of Si1-xGex Gate Stacks for High Performance Dual Channel CMOS**
Oct. 27 **(Invited)** ChoongHyun Lee, Richard G. Southwick III, Shogo Mochizuki, Paul Jamison, Ruqiang Bao, *Rajan Pandey, *Aniruddha Konar, Takashi Ando, Vijay Narayanan, Bala Haran, Hemanth Jagannathan
Jade Room 3
IBM Research, USA; *GLOBALFOUNDRIES Inc.
- 14:00** **SD4-2** **Performance Improvement of InGaAs FinFET Using NH3 Treatment**
Oct. 27 **(Invited)** Edward Yi Chang, Quang-Ho Luc, Huy-Binh Do, Yueh-Chin Lin
Jade Room 3
National Chiao Tung University, Taiwan

14:30	SD4-3	Layer thinning of MoS2 flakes by thermal annealing in air
Oct. 27		Qiyuan Wang, Youwei Zhang, Chunxiao Cong, Laigui Hu, Pengfei Tian, Ran Liu, Zhi-jun Qiu
	Jade Room 3	Fudan University, China
14:45	SD4-4	Dynamic Characteristics and Related Trapping Effects of GaN-based Fin-MISHEMTs
Oct. 27		Xingye Zhou, Xin Tan, Yuanjie Lv, Yuangang Wang, Xubo Song, Guodong Gu, Peng Xu, Hongyu Guo, Zhihong Feng, and Shujun Cai
	Jade Room 3	Hebei Semiconductor Research Institute, China
15:00	SD4-5	Analytical Model of Internal Heat Transfer of a Power Chip with Through Silicon Via
Oct. 27		Jingyu Liu, Yongyong Wang, Xunyong Yang, Fashun Yang, Kui Ma
	Jade Room 3	Guizhou University, China
15:15	SD4-6	Surface Effect on the Current-Voltage Characteristics of Back-Gated MoS2 Channel MOSFET
Oct. 27		Mingyue He, Sitong Bu, Daming Huang
	Jade Room 3	Fudan University, China

Coffee Break

SA5 Special Session: Sensory Circuits and Systems

Session Chair: Guoxing Wang, Shanghai Jiaotong University, China

15:45	SA5-1	Low Complexity and Low Power Multiplierless FIR Filter Implementation
Oct. 27	(Invited)	Xin Lou, Wenbin Ye
	Sapphire Room	ShanghaiTech University, China
16:15	SA5-2	Dual-pulse Nonlinear Photoacoustic Imaging: Physics, Sensing and Imaging System Design
Oct. 27	(Invited)	Fei Gao, Xiaohua Feng, Ruochong Zhang, Siyu Liu, Ran Ding, Yuanjin Zheng
	Sapphire Room	ShanghaiTech University, China
16:45	SA5-3	Ultrathin Flexible Coils for Wireless Power and Data Link in Biomedical Sensors
Oct. 27	(Invited)	Wei Xu, Tianyuan Cheng, Chundong Wu, Nanshu Lu, Zeyu Yang, Yong Lian, Guoxing Wang
	Sapphire Room	Shanghai Jiao Tong University, China
17:15	SA5-4	An APWM Controlled LLC Resonant Converter for a Wide Input Range and Different Load Conditions
Oct. 27	(Invited)	Zhongxia Shang, Yang Zhao, Yong Lian
	Sapphire Room	York University, Canada

SB5 High speed Data Converter

Session Chair: Fan Ye, Fudan University, China

15:45	SB5-1	A Low-Power On-Chip Calibration Technique for Pipelined ADCs
Oct. 27	(Invited)	Xizhu Peng, Zuowei Mao, Ang Gao, Laishen Che, He Tang
	Jade Room 1	University of Electronic Science and Technology of China, China
16:15	SB5-2	A 6-bit 700-MS/s single-channel SAR ADC with low kickback noise comparator in 40-nm CMOS
Oct. 27		Long Zhao, Bao Li, Yuhua Cheng
	Jade Room 1	Peking University, China
16:30	SB5-3	A Power-Efficient Reconfigurable Two-Step VCO-Based ADC for

Software-Defined Radio

- Oct. 27
Jade Room 1
16:45 SB5-4 **Xinpeng Xing, Peng Zhu, Hui Liu, Wei Wang, Georges Gielen**
A High-Resolution Pipeline Time-to-Digital Converter in 0.18 μ m CMOS Technology
Tsinghua University, China
- Oct. 27
Jade Room 1
17:00 SB5-5 **Wang Yongsheng, Ye Qiao, Zhao Han, Liu Xiaowei**
A 14bit 320MS/s pipelined-SAR ADC based on multiplexing of dynamic amplifier
Harbin Institute of Technology, China
- Oct. 27
Jade Room 1
17:15 SB5-6 **Honghao Chu, Fule Li**
All-Digital background calibration technique of the channel-time-mismatch in a two-channel TIADC
Tsinghua University, China
- Oct. 27
Jade Room 1
17:30 SB5-7 **Sujuan Liu, Ze Li, Zhenzhen Zhao, Yihui Fan**
A Reference Signal Phase Independent High Precision Timing Skew Mismatch Estimation Scheme for Time Interleaved ADC
Beijing University of Technology, China
- Oct. 27
Jade Room 1
Ruwu Xiao, Qiyang Lei, Xuan Guo, Yuping Zhao
Peking University, China

SC5 VLSI for Emerging Applications

Session Chair: Zou Zhuo, Fudan University, China

- 15:45 SC5-1** **A Pseudo MMSE Linear Equalizer for 60GHz Single Carrier Baseband Receiver**
Oct. 27 **(Invited)** **Hsun-Wei Chan, Chang-Ting Wu, Chih-Wei Jen, Chun-Yi Liu, Wei-Che Lee, Shyh-Jye Jou**
Jade Room 2
National Chiao-Tung University, Taiwan
- 16:15 SC5-2** **Highly-reliable Integrated Circuits for Ground and Space Applications**
Oct. 27 **(Invited)** **Kazutoshi Kobayashi**
Jade Room 2
Kyoto Institute of Technology, Japan
- 16:45 SC5-3** **Object-recognition VLSI for pedestrian detection in automotive applications**
Oct. 27 **(Invited)** **Fengwei An, Xiangyu Zhang, Lei Chen, Idaku Ishii**
Jade Room 2
Hiroshima University, Japan
- 17:15 SC5-4** **A Cluster-Scalable VLIW Cryptography Processor with High Performance and Energy Efficiency**
Oct. 27 **Wei Huang, Zhonghe Guo, Xiaohua Song, Fei Sun**
Jade Room 2
State Key Lab of Cryptology, China
- 17:30 SC5-5** **A Novel Low-cost FPGA-based Real-time Object Tracking System**
Oct. 27 **Peng Gao, Ruyue Yuan, Zhicong Lin, Linsheng Zhang, Yan Zhang**
Jade Room 2
Harbin Institute of Technology, China

SD5 Reliability in New Devices

Session Chair: Xiaoxu Kang, Shanghai IC R&D Center, China

- 15:45 SD5-1** **Hot carrier reliability in LDMOS devices**
Oct. 27 **(Invited)** **Jifa Hao**
Jade Room 3
ON Semiconductor, USA
- 16:15 SD5-2** **The enhancement mode AlGaN/GaN high electron mobility transistor based on charge storage**
Oct. 27 **(Invited)** **Hui Wang, Lingli Jiang, Ning Wang, Xinpeng Lin, Hongyu Yu**

Jade Room 3		Southern University of Science and Technology, China
16:45	SD5-3	Hot Carrier Reliability in Ultra-Scaled SiGe Channel p-FinFETs
Oct. 27	(Invited)	Miaomiao Wang, Xin Miao, James H Stathis, Richard Southwick
Jade Room 3		IBM, USA
17:15	SD5-4	Hot carrier aging of nano-scale devices: characterization method, statistical variation, and their impact on use voltage
Oct. 27	(Invited)	Jian F. Zhang, Meng Duan, Zhigang Ji, Weidong Zhang
Jade Room 3		Liverpool John Moores University, UK
17:45	SD5-5	Independent Band Modulation in Two-Dimensional van der Waals Heterostructure Based on a New Device Architecture
Oct. 27	(Invited)	Zhongxun Guo, Wu Zan, Hu Xu, Fuyou Liao, Lin Chen, Hao Zhu, Qingqing Sun, Shijin Ding, Peng Zhou, Wenzhong Bao, David Wei Zhang
Jade Room 3		Fudan University, China

Oct. 27 17:45-18:45

Poster Session 2

	P2-01	TSV modelling in 3D IC thermoelectric simulation
Oct. 27		Tongyang Ye, Ligang Hou, Shier Zhang, Jinhui Wang, Xiaohong Peng Beijing University of Technology, China
	P2-02	Low Power Mapping Optimization of Loops for Dual-Vdd CGRAs
Oct. 27		Kaijian Yuan, Xingming Zhang National Digital Switching System Engineering & Technological Research Center, China
	P2-03	A 15MHz BW Continuous-Time $\Delta\Sigma$ Modulator with High Speed Digital ELD Compensation
Oct. 27		Hang Hu, Manxin Li, Zhiyuan Dai, Fan Ye, Junyan Ren Fudan University, China
	P2-04	An Inductorless Noise-Cancelling CMOS LNA Using Wideband Linearization Technique
Oct. 27		Benqing Guo, Jun Chen, Hongpeng Chen, Xuebing Wang, Chang Liu University of Electronic Science and Technology of China, China
	P2-05	Design and Realization of a X-band Graphene Amplifier MMIC
Oct. 27		Xubo Song, Cui Yu, Zezhao He, Qingbin Liu, Tingting Han, Shaobo Dun, Yuanjie Lv, Shujun Cai, Zhihong Feng Hebei Semiconductor Research Institute, China
	P2-06	Ultra Low Loss and High Linearity RF Switch using 130nm SOI CMOS Process
Oct. 27		Hongwei Zhu, Qiuliang Li, Hao Sun, Zhipeng Wang, Ran Liu, Yi Liu Fudan University, China
	P2-07	A Novel Positive-feedback Read Scheme with tail current source of STT-MRAM
Oct. 27		Jin Yan, Dongsheng Liu, Xuecheng Zou, Bangdi Xu Huazhong University of Science and Technology, China
	P2-08	A Single-Inductor MIMO Buck-Boost Converter with Inductor-Peak-Current PFM Control for Multiple Energy Harvesting
Oct. 27		Chen Jiao, Zunchao Li, Chuang Wang, Lvchen Zhou, Hailong Bai Xi'an Jiaotong University, China
	P2-09	An Area-Efficient Interconnection Network for Coarse-Grain Reconfigurable

Cryptographic Array

- Oct. 27 Tongzhou Qu, Zibin Dai, Longmei Nan, Wei Li, Anqi Yin
Institute of Information Science and Technology, China
- P2-10** **Extraction of Circuit Transfer Functions with SuTra Analyses**
- Oct. 27 Sotoudeh Hamedi-Hagh
San Jose State University, USA
- P2-11** **A Force Directed Partitioning Algorithm for 3D Floorplanning**
- Oct. 27 Linqun Lyu, Takeshi Yoshimura
Waseda University, Japan
- P2-12** **A Broadband Power Detector with Temperature and Process Compensation**
- Oct. 27 Yifan Gao, Weigang Xu, Chenyang Kong, Zhangwen Tang
Fudan University, China
- P2-13** **Type-3 2-D Multimode IIR Filter Architecture and the Corresponding Symmetry Filter's Error Analysis**
- Oct. 27 Pei-Yu Chen, Lan-Da Van, I. H. Khoo, Hari C. Reddy
National Chiao Tung University, Taiwan
- P2-14** **A Self-Adaptive Digital Calibration Technique for Multi- Channel High Resolution Capacitive SAR ADCs**
- Oct. 27 Binbin Lyu, Wengao Lu, Sijia Yang, Zhongjian Chen, Yacong Zhang
Peking University, China
- P2-15** **Design and Implementation of High-speed Configurable ECC Co-processor**
- Oct. 27 Ze He, Xiaowen Chen
National University of Defense Technology, China
- P2-16** **A Metastability-Based True Random Number Generator on FPGA**
- Oct. 27 Chaoyang Li, Qin Wang, Jianfei Jiang, Nin Guan
Shanghai Jiao Tong University, China
- P2-17** **A Signal Noise Separation Method for the Instant Mixing Linear and Nonlinear Circuits with MISEP Algorithm**
- Oct. 27 Liwen Zhu, Xiaole Cui, Xiang Li, Xiaoxin Cui
Peking University, China
- P2-18** **A Design of High Performance Full Adder with Memristors**
- Oct. 27 Kuimin Zhang, Xiaole Cui, Xiaoxin Cui
Peking University, China
- P2-19** **An input buffer for 12bit 2GS/s ADC**
- Oct. 27 Fubiao Cao, Yongzhen Chen, Fan Ye, Junyan Ren
Fudan University, China
- P2-20** **A Proved Dither-injection Method for Memory Effect in Double Sampling Pipelined ADC**
- Oct. 27 Fubiao Cao, Yongzhen Chen, Yuefeng Cao, Fan Ye, Junyan Ren
Fudan University, China
- P2-21** **A High Performance Switched-Capacitor Programmable Gain Amplifier Design in 0.18 μ m CMOS Technology**
- Oct. 27 Shuang Cui, Tianzhao Liu, Haoran Gong, Bingyan Hu, Yuchun Chang
Jilin University, China
- P2-22** **High Voltage Charge Pump Circuit Using Vertical Parallel Plate Capacitors**
- Oct. 27 Liang Zhang, Xu Cheng, Tong xiaodong, Xianjin Deng
China Academy of Engineering Physics, China
- P2-23** **A 14-bit 5 MS/s Split Non-binary SAR ADC**
- Oct. 27 Shu Yang, Minghang Liu, Yusong Mu, Yuchun Chang

- Jin Lin University, China
- Oct. 27 **P2-24** **A Clock Interpolation Structure Using DLL for Clock Distribution in ADC**
Shijia Zhu, Yu Wang, Fan Ye, Jun Xu
Fudan University, China
- Oct. 27 **P2-25** **A Radiation-hard Waffle Layout for BCD Power MOSFET**
Xiao Zhou, Ping Luo, Linyan He, Tiancheng Xiao
University of Electronic Science and Technology of China, China
- Oct. 27 **P2-26** **A 18 mW 12 bit 50 MS/s SHA-less Pipelined ADC**
Weigang Xu, Yifan Gao, Xiaodong Liu, Zhangwen Tang
Fudan University, China
- Oct. 27 **P2-27** **A 16-bit two-step pixel-level ADC for 384*288 Infrared Focal Plane Array**
Sijia Yang, Lingzi Luo, Wengao Lu, Guangyi Shi, Binbin Lyu, Yuze Niu, Yacong Zhang, Zhongjian Chen
Peking University, China
- Oct. 27 **P2-28** **A Hybrid Fault Model for Differential Fault Attack on AES**
Yixia Liu, Xiaoxin Cui, Jian Cao, Xing Zhang
Peking University, China
- Oct. 27 **P2-29** **Design and Implementation of Homogeneous Multi-core System**
Xiaolei Wang, Dongming Qu, Yukun Song, Duoli Zhang
Hefei University of Technology, China
- Oct. 27 **P2-30** **A Chain-Multiplier for Large Scale Matrix Multiplication**
Can Wei, Yukun Song, Duoli Zhang
Hefei University of Technology, China
- Oct. 27 **P2-31** **Joint Detection and Decoding for Polar-Coded OFDM-IDMA Systems**
Xiangyun Deng, Jin Sha, Xiaotian Zhou, Xiaohu You, Chuan Zhang
Southeast University, China
- Oct. 27 **P2-32** **A High-Speed Low-Power Charge Pump with Dynamic Current Matching**
Licheng Xu, Xinchu Gao, Jing Jin
Shanghai Jiao Tong University, China
- Oct. 27 **P2-33** **A Passive Mixer-First Receiver with Negative Feedback for Impedance Matching**
Shaoqin Yao, Litong Liu, Jing Jin
Shanghai Jiao Tong University, China
- Oct. 27 **P2-34** **A Novel Equivalent Circuit Model of the Surge Wave Generator**
Yukuai Chen, Jian Cao, Yuan Wang, Xing Zhang, Guangyi Lu
Peking University, China
- Oct. 27 **P2-35** **Designing Hardware Trojans and Their Detection based on a SVM-based Approach**
Tomotaka Inoue, Kento Hasegawa, Masao Yanagisawa, Nozomu Togawa
Waseda University, Japan
- Oct. 27 **P2-36** **A Light-Weight Energy-Efficient Resilient Circuit for Variation Tolerance**
Xiaopei Chen, Xiaoyan Xiang, Chen Chen, Jianyi Meng, Sheng Wang
Fudan University, China
- Oct. 27 **P2-37** **Design of Ka band bandpass filter using Silicon Micromachined technology**
Qiulong Hong, Xiubo Liu, Shaodong Wang
Hebei Semiconductor Research Institute, China
- Oct. 27 **P2-38** **Physics based Compact Model of GaN HEMT with an Efficient Parameter Extraction Flow**
Hao Zhang, Ahmed Raslan, Slim Boumaiza, Lan Wei
University of Waterloo, Canada

- P2-39** **CMOS 0.35 μ m Implementation of Time-Domain Measurement of Resonator's Quality Factor**
 Oct. 27 Xiaojiao Ren, Ming Zhang, Nicolas Llaser
 University PARIS 11, France
- P2-40** **A 1.2V Output RF Energy Harvester with a Harvesting-Efficiency Tracking circuit**
 Oct. 27 Xiaofei Hu, Xiao Ge, Ting Yi, Danzhu Lv, Zhiliang Hong
 Fudan University, China
- P2-41** **A 12bit Asynchronous SAR-Incremental Sub-range ADC**
 Oct. 27 Manxin Li, Hang Hu, Zhiyuan Dai, Fan Ye, Junyan Ren
 Fudan University, China
- P2-42** **A Scalable Hardware Architecture for Multi-Layer Spiking Neural Networks**
 Oct. 27 Zhaozhong Ying, Chong Luo, Xiaolei Zhu
 Zhejiang University, China
- P2-43** **32-channel ROIC for X-ray Imaging System**
 Oct. 27 Dan Liu, Feng Gao, Liguang Hao, Jianxin Liao
 The First Research Institute of Ministry of Public Security, China
- P2-44** **A High Performance Real-Time Edge Detection System with NEON**
 Oct. 27 Kaixuan Zhang, Li Ding, Yujie Cai, Wenbo Yin, Fan Yang, Jun Tao, Lingli Wang
 Fudan University, China
- P2-45** **Demonstrate High ROFF/RON Ratio and Forming-Free RRAM for rFPGA Application based on Switching Layer Engineering**
 Oct. 27 Wenfeng Dong, Dong Liu, Shun Xu, Bing Chen, Yi Zhao
 Zhejiang University, China
- P2-46** **Power Optimization on MUX Mapped Circuits**
 Oct. 27 Zhiwen Chen, Hui-hong Zhang
 Ningbo University, China
- P2-47** **A 40nm 512Kb Dual-Port SRAM Macro with Hybrid Dual Power Supply Scheme for Low Power SoCs**
 Oct. 27 Zhao-Yong Zhang, Wei-Chang Wang, Shuang Lv, Biao Chen
 Faraday Technology Corporation, China
- P2-48** **Active Ego-noise Control Based on Metamaterial in Small-size Robot**
 Oct. 27 Xihan Gu, Yun Chen, Xiaofeng Wu
 Fudan University, China
- P2-49** **Genetic Algorithm Based on Divide-and-Conquer Strategy for Defect-Tolerant CMOL Mapping**
 Oct. 27 Xiaojing Zha, Yinshui Xia
 Ningbo University, China
- P2-50** **Application of LDPC Codes on PUF Error Correction Based on Code-offset Construction**
 Oct. 27 Kai Sun, Yingjie Lao, Weiqiang Liu, Xiaohu You, Chuan Zhang
 Southeast University, China
- P2-51** **High Speed, Low Offset, Low Power Differential Comparator with Constant Common Mode Voltage**
 Oct. 27 Mehdi Nasrollahpour, Sotoudeh Hamedi-Hagh
 San Jose State University, USA
- P2-52** **A Programmable Divider with Extended Division Range for 24GHz FMCW Frequency Synthesizer**
 Oct. 27 Yuanyuan Xu, Wei Li, Dan Wu, Ning Li
 Fudan University, China
- P2-53** **A Capacitor-less LDO With Transient-Response Improvement**

- Oct. 27 Pengfei Liao, Hao Chen, Lin Tan, Liang Zhou, Fan Liu, Luncai Liu
Sichuan Institute of Solid-State Circuits, China
- P2-54** **Large-Area High-Density Active Microelectrodes Array for Neural Signal Recording Based on CMOS Circuit**
- Oct. 27 Weiye Cai, Hongge Li
BeiHang University, China
- P2-55** **DC MUX PUF: A Highly Reliable Feed-Back MUX PUF Based on Measuring Duty Cycle**
- Oct. 27 Yunhao Xu, Yingjie Lao, Weiqiang Liu, Xiaohu You, Chuan Zhang
Southeast University, China
- P2-56** **The D-band MMIC LNA circuit using 70nm InP HEMT Technology**
- Oct. 27 Yutong Wang, Hongjiang Wu, Jing Li, Xingchang Fu
The 13th Research Institute of CHINA Electronics Technology Group Corporation, China
- P2-57** **FPGA-based Convolution Neural Network for Traffic Sign Recognition**
- Oct. 27 Yuchen Yao, Zhiqian Zhang, Zhen Yang, Jian Wang, Jinmei Lai
Fudan University, China
- P2-58** **A Digital-Assistant Time-to-Amplitude Converter with Dynamic Range Improvement**
- Oct. 27 Zengxin Liu, Shaowei Zhen, Shuiqing Xi, Xinjiang Gao, Lei Yang, Jiongwei Zheng, He Tang, Yajuan He, Ping Luo, Bo Zhang
University of Electronic Science and Technology, China
- P2-59** **The Implement of Digital Front End in All-Digital Quadrature RF Transmitter**
- Oct. 27 ChenYang Wang, Yilei Shen, Pan Xue, Zhiliang Hong
Fudan University, China
- P2-60** **Efficient Fast Convolution Architectures for Convolutional Neural Network**
- Oct. 27 Weihong Xu, Zhongfeng Wang, Xiaohu You, Chuan Zhang
Southeast University

Technical Session

Saturday, Oct. 28

Keynote Speech K3-1 & K3-2

- 8:30-9:15 K3-1 NanoBridge FPGA for IoT era**
Oct. 28 **(Keynote)** Dr. Yukihide Tsuji
GrandBall Room System Platform Research labs. NEC corp., Japan
- 9:15-10:00 K3-2 Energy-Quality Scalable Integrated Circuits and Systems – Continuing the Energy Scaling in spite of Moore’s Law**
Oct. 28 **(Keynote)** Prof. Massimo Alioto,ECE
GrandBall Room National University of Singapore, Singapore

SA6 Special Session: Low Power Digital Circuits

Session Chair: Yajun Ha, ShanghaiTech University, China

- 10:15 SA6-1 Metallic-Carbon-Nanotube-Removal Tolerant SRAM Cell with 9 Transistors**
Oct. 28 **(Invited)** Yanan Sun, Weifeng He, Zhigang Mao, Hailong Jiao, Volkan Kursun
Sapphire Room Shanghai Jiao Tong University, China
- 10:45 SA6-2 Analysis and Design of Energy-Efficient Data-Dependent SRAM**
Oct. 28 **(Invited)** Wenfeng Zhao, Ang Li, Yi Wang, Yajun Ha
Sapphire Room University of Minnesota, USA
- 11:15 SA6-3 Low-Power Single-Phase Clocked Redundant-Transition-Free Flip-Flop Design with Conditional Charging Scheme**
Oct. 28 **(Invited)** Ling Chen, Yanan Sun, Weifeng He
Sapphire Room Shanghai Jiao Tong University, China
- 11:45 SA6-4 Near-Threshold Processor Design Techniques for Power-Constrained Computing Devices**
Oct. 28 **(Invited)** Jun Zhou, Tony Tae-Hyoung Kim, Yong Lian
Sapphire Room University of Electronic Science and Technology of China, China

SB6 Power Conversion and Management

Session Chair: Lin Cheng, University of Science and Technology, Hong Kong

- 10:15 SB6-1 Optimization compensation for Primary-Side-Regulated Flyback Converters in Continuous-Conduction-Mode and Discontinuous Conduction Mode**
Oct. 28 **(Invited)** Gong Xiaowu
Jade Room 1 Infineon Technologies Asia Pacific Pte Ltd, Singapore
- 10:45 SB6-2 Recent Progress in GaN Devices for Power and Integrated Circuit**
Oct. 28 **(Invited)** Nobuyuki Otsuka, Yasufumi Kawai, Shuichi Nagai
Jade Room 1 Panasonic, Japan
- 11:15 SB6-3 A high-precision voltage regulator with dynamic load technique and overcurrent protection**
Oct. 28 Zekun Zhou, Yue Shi
Jade Room 1 University of Electronic Science and Technology of China, China

11:30 SB6-4 Backscattering in Multicycle Q-modulation for Bio-Implants Wireless Power Transfer
Oct. 28 Yang Liu, Bin Li, Mo Huang, Zhaoquan Chen
Jade Room 1 South China University of Technology, China

11:45 SB6-5 A Single Inductor Tri-Input Dual-Output Buck-Boost DC-DC Converter with MPPT for Multi-Source Energy Harvesting
Oct. 28 Xiao Ge, Xiaofei Hu, Yajie Qin, Zhiliang Hong
Jade Room 1 Fudan University, China

SC6 Low-power SoCs

Session Chair: Na Yan, Fudan University, China

10:15 SC6-1 A High Utilization FPGA-Based Accelerator for Variable-Scale Convolutional Neural Network
Oct. 28 Xin Li, Yujie Cai, Jun Han, Xiaoyang Zeng
Jade Room 2 Fudan University, China

10:30 SC6-2 A Novel Mixed Reconfigurable System on Chip Based on Field Programmable Analog Array
Oct. 28 Lintao Liu, Yuhan Gao, Haoming Du
Jade Room 2 CETC, China

10:45 SC6-3 Parallel Implementations of SHA-3 on a 24-core Processor with Software and Hardware Co-Design
Oct. 28 Jianwei Yang, Weizhen Wang, Zhicheng Xie, Jun Han, Zhiyi Yu, Xiaoyang Zeng
Jade Room 2 Fudan University, China

11:00 SC6-4 A 3600 x 3600 Large-scale ISFET Sensor Array for High-throughput pH Sensing
Oct. 28 Yongxin Cong, Dongping Wu
Jade Room 2 Fudan University, China

11:15 SC6-5 Uniform Belief Propagation Processor for Massive MIMO Detection and GF(2ⁿ) LDPC Decoding
Oct. 28 Shusen Jing, Anlan Yu, Xiao Liang, Xiaohu You, Chuan Zhang
Jade Room 2 Southeast University, China

11:30 SC6-6 Design of Router for Spiking Neural Networks
Oct. 28 Yewen Ni, Xiaoxin Cui, Yuanning Fan, Qiankun Han, Xiaole Cui
Jade Room 2 Peking University, China

11:45 SC6-7 A Fuel Injection Control SoC for Diesel Engine Management System
Oct. 28 Qinmiao Kang, Ming Zhou
Jade Room 2 Tsinghua University, China

SD6 CAD (3)

Session Chair: Ngai Wong, University of Hong Kong, HK

10:15 SD6-1 Efficient Algorithms for Resistance and Capacitance Calculation Problems in the Design of Flat Panel Display
Oct. 28 **(Invited)** Wenjian Yu, Taotao Lu
Jade Room 3 Tsinghua University, China

10:45 SD6-2 Characterization of Single-Crystalline Graphene ESD Interconnects
Oct. 28 **(Invited)** Qi Chen, Cheng Li¹, Fei Lu¹, Chenkun Wang¹, Feilong Zhang¹, Tianru Wu², Xiaoming Xie², Kun Zhang², Xinxin Li², Jimmy Ng³, Ya-Hong Xie³, Yuhua Cheng⁴ and Albert Wang^{1*}
Jade Room 3 University of California-Riverside, USA

11:15	SD6-3	Compact Modeling Approach for Electro-Mechanical System Simulation
Oct. 28	(Invited)	T.K. Maiti, D. Navarro, M. Miura-Mattausch, H. J. Mattausch
Jade Room 3		Hiroshima University, Japan
11:45	SD6-4	Short Path Padding with Multiple-Vt cells for Wide-Pulsed-Latch Based Circuits at Ultra-Low Voltage
Oct. 28		Yongming Ding, Wei Jin, Guanghui He, Weifeng He
Jade Room 3		Shanghai Jiao Tong University, China
12:00	SD6-5	A Fast HDL Model for Full-Custom FPGA Verification
Oct. 28		Kaixuan Zhang, Zhihua Feng, Hao Zhou
Jade Room 3		Fudan University, China

Coffee Break

SA7 Sensors and Display

	Session Chair:	Yuan Gao, University of Science and Technology, Hong Kong
13:30	SA7-1	Effects of Device Structures on Piezoresistive Behaviors of PEDOT: PSS Pressure Sensors
Oct. 28	(Invited)	Jer-Chyi Wang
Sapphire Room		Chang Gung University, Taiwan
14:00	SA7-2	Micro-LED arrays for display and communication: device structure and driver architecture
Oct. 28	(Invited)	Kiat Seng Yeo, Wen Xian Ng, Mei Yu Soh, T. Hui Teo
Sapphire Room		Singapore University of Technology and Design, Singapore
14:30	SA7-3	A biomedical microfluidic mixer in MEMS application Using Inkjet
Oct. 28		Robert K.F. Teng, Qian Hou, Jun chen, Zhanjiang Guo, Zeng Peng, Yuheng Nie
Sapphire Room		California State University, USA
14:45	SA7-4	A Bulk-driven Pixel Circuit with Wide Data Voltage Range for OLEDs Microdisplays
Oct. 28		Huiyuan Lu, Hongge Li
Sapphire Room		BeiHang University, China
15:00	SA7-5	A Low-Power Self-Calibration Digital-Output CMOS Temperature Sensor with $\pm 0.1^\circ\text{C}$ Inaccuracy from -40°C to 85°C
Oct. 28		Yuze Niu, Wengao Lu, Yacong Zhang, Shanzhe Yu, Zhongjian Chen
Sapphire Room		Peking University, China
15:15	SA7-6	A 58-dB SNDR 1.32-mW Chopper-Stabilized Analog Front-End for Graphene Hall Element Detecting Application
Oct. 28		Chengying Chen, Liming Chen, Zhenli Lai
Sapphire Room		Xiamen University of Technology, China

SB7 RF Design Techniques (2)

	Session Chair:	Yumei Huang, Fudan University, China
13:30	SB7-1	RF Mixer Design Techniques Using GaAs Process
Oct. 28	(Invited)	Jinna Yan, Bharatha Kumar Thangarasu, Kiat Seng Yeo
Jade Room		Singapore University of Technology and Design, Singapore
14:00	SB7-2	5G FEM Design with Advanced SOI Process
Oct. 28	(Invited)	Chaojiang Li, Min Wang, Taiyun Chi, Arvind Kumar, Myra Boenke, Dawn Wang, Ned Cahoon, Anirban Bandyopadhyay, Alvin Joseph, Hua Wang
Jade Room		Globalfoundries, USA
14:30	SB7-3	Ultrafast Spintronic Integrated Circuits

Oct. 28 **(Invited)** Jiaqi Wei, Liang Chang, Zhaohao Wang, Xiaoyang Lin, Kaihua Cao, Hushan Cui, Wang Kang, Haoxuan Chen, Lang Zeng, Youguang Zhang, Chao Zhao, Weisheng Zhao
Jade Room Beihang University, China

15:00 SB7-4 Ultra-High-Data-Rate 60-GHz CMOS Transceiver for Future Radio Access Network

Oct. 28 **(Invited)** Rui Wu, Ryo Minami, Yuuki Tsukui, Seitaro Kawai, Yuuki Seo, Shinji Sato, Kento Kimura, Satoshi Kondo, Tomohiro Ueno, Nurul Fajri, Shoutarou Maki, Noriaki Nagashima, Yasuaki Takeuchi, Tatsuya Yamaguchi, Ahmed Musa, Korkut Kaan Tokgoz, Teerachot Siriburanon, Bangan Liu, Yun Wang, Jian Pang, Ning Li, Masaya Miyahara, Kenichi Okada, and Akira Matsuzawa
Jade Room Tokyo Institute of Technology, Japan

SC7 (Special Session) Neural Network: Efficient Implementations and Applications

Session Chair: Chuan Zhang, Southeast University, China

13:30 SC7-1 Neural Networks: Efficient Implementations and Applications

Oct. 28 **(Invited)** Chuan Zhang, Weihong Xu
Jade Room 2 Southeast University, China

13:40 SC7-2 Using Fermat Number Transform to Accelerate Convolutional Neural Network

Oct. 28 **(Invited)** Weihong Xu, Xiaohu You, and Chuan Zhang
Jade Room 2 Southeast University, China

14:05 SC7-3 A Layer-based Structured Design of CNN on FPGA

Oct. 28 Chao Huang, Siyu Ni, Gengsheng Chen
Jade Room 2 Fudan University, China

14:30 SC7-4 Automatic Classification of Leukocytes Using Deep Neural Network

Oct. 28 **(Invited)** Wei Yu, Jing Chang, Cheng Yang, Limin Zhang, Han Shen, Yongquan Xia, Jin Sha
Jade Room 2 Nanjing University, China

14:55 SC7-5 Energy Efficient SVM Classifier Using Approximate Computing

Oct. 28 **(Invited)** Yangcan Zhou, Jun Lin, Zhongfeng Wang
Jade Room 2 Nanjing University, China

SD7 New Devices and Advanced Technologies (4)

Session Chair: Chunxiao Cong, Fudan University, China

13:30 SD7-1 Ultra low power and high performance nanoelectronic devices

Oct. 28 **(Invited)** Francis Balestra
Jade Room 3 Grenoble INP/CNRS, France

14:00 SD7-2 High performance transistors based on two dimensional materials

Oct. 28 **(Invited)** Mingqiang Huang, Xiong Xiong, Tiaoyang Li, Yanqing Wu
Jade Room 3 Huazhong Univ. of Science and Technology, China

14:30 SD7-3 NiGe Metal Source/Drain Ge pMOSFETs for Future High Performance VLSI Circuits Applications

Oct. 28 **(Invited)** Rui Zhang, Jinghui Han, Junkang Li, Xiaoyu Tang, Yi Zhao
Jade Room 3 Zhejiang University, China

15:00 SD7-4 Deeply Scaled VLSI Analog Transistor Design and Optimization

Oct. 28 **(Invited)** Jason C.S. Woo, Peng Lu, Po-Yen Chien, Xicheng Duan
Jade Room 3 University of California, Los Angeles, USA

Coffee Break

SA8 Low Power VLSI for Communication

Session Chair: Yun Chen, Fudan University, China

- 15:45 SA8-1** **Toward Real-time 3D Modeling System with Cubic-Millimeters Wireless Sensor Nodes**
Oct. 28 **(Invited)** Masanori Hashimoto, Ryo Shirai, Yuichi Itoh, Tetsuya Hirose
Sapphire Room Osaka University, Japan
- 16:15 SA8-2** **Joint Detection and Decoding for Non-Binary LDPC Coded MIMO Systems**
Oct. 28 Yiqian Cai, Jin Sha, Shusen Jing, Xiaohu You, Chuan Zhang
Sapphire Room Nanjing University, China
- 16:30 SA8-3** **The VLSI Architecture for Channel Estimation Based on ADMA**
Oct. 28 Xiaozhen Liu, Hongxiang Xie, Jin Sha, Feifei Gao, Shi Jin, Xiaohu You, Chuan Zhang
Sapphire Room Nanjing University, China
- 16:45 SA8-4** **An Efficient Successive Cancellation Polar Decoder Based on New Folding Approaches**
Oct. 28 Xiao Liang, Yechao She, Harish Vangala, Xiaohu You, Chuan Zhang, Emanuele Viterbo
Sapphire Room Southeast University, China
- 17:00 SA8-5** **RC6 Architecture-Adaptive Implementation for Coarse-Grained Reconfiguration Array**
Oct. 28 Anqi Yin, Zibin Dai, Longmei Nan, Wei Li
Sapphire Room PLA Information Engineer University, China
- 17:15 SA8-6** **DRFNet: A Lightweight and High Accuracy Network for Resource-limited Implementation**
Oct. 28 Hengliang Xiang, Liang Chen, Wei Xu
Sapphire Room Fudan University, China
- 17:30 SA8-7** **Design of Digital Control Unit for Implantable Stimulator Chip**
Oct. 28 Guoqing Sun, Xiaohong Peng, Jun Zhao, Rui Wang, Xiaodan Li
Sapphire Room Beijing University of technology, China

SB8 RF Design Techniques (3)

Session Chair: Yann Deval, University of Bordeaux, France

- 15:45 SB8-1** **Digital RF transmitter architectures exploiting FIRDACs in various configurations**
Oct. 28 **(Invited)** Andreas Kaiser, Antoine Frappe
Jade Room 1 Univ. Lille, France
- 16:15 SB8-2** **Terahertz CMOS Transceiver for Tera-bps Wireless Link**
Oct. 28 **(Invited)** Minoru Fujishima
Jade Room 1 Hiroshima University, Japan
- 16:45 SB8-3** **125KHz Wake-up Receiver and 433MHz Data Transmitter for Battery-less TPMS**
Oct. 28 Qinmiao Kang, Ming Zhou
Jade Room 1 Tsinghua University, China
- 17:00 SB8-4** **A Low Power High Integrated BLE Transceiver**
Oct. 28 Zhang Cuncai, Zhao Hui, Liang Jie
Jade Room 1 Nationz Technologies Inc, China
- 17:15 SB8-5** **A Low-Power Digital GFSK Receiver with Mid-value Filtering Frequency Offset**

Estimator and Soft Anti-Overlap Slicer

Oct. 28		Yu Li, Ziqian Wang, Song Chen, Fujiang Lin
Jade Room 1		University of Science and Technology of China (USTC), China
17:30	SB8-6	A 1.0-3.0GHz LTE Transmitter with CIM Enhancement
Oct. 28		Yun Yin, Tong Li, Xiaoyong Xue
Jade Room 1		Fudan University, China

SC8 Circuit and Systems for IoT

Session Chair: Lan Wei, University of Waterloo, Canada

15:45	SC8-1	Tensor-Network-Based Predistorter Design for Multiple-Input Multiple-Output Nonlinear Systems
Oct. 28	(Invited)	Cong Chen, Kim Batselier, Mihai Telescu, Stephane Azou, Noel Tanguy, Ngai Wong
Jade Room 2		University of Hong Kong, HK
16:15	SC8-2	Towards An LC Passive Wireless Sensor Platform
Oct. 28	(Invited)	Qing-An Huang, Lei Dong, Li-Feng Wang
Jade Room 2		Southeast University, China
16:45	SC8-3	Design and Development of a Self-contained and Non-Invasive Integrated System for Electricity Monitoring Applications
Oct. 28		Sid Zarabi, Egon Fernandes, Armaghan Salehian, David Nairn, Lan Wei
Jade Room 2		University of Waterloo, Canada
17:00	SC8-4	Integrating Operation Scheduling and Binding for Functional Unit Power-Gating in High-Level Synthesis
Oct. 28		Nan Wang, Hengxiao Wang, Yue Jin, Jiongyao Ye
Jade Room 2		School of Information Science and Engineering, ECUST, China
17:15	SC8-5	New 2-D Quadrantal- and Diagonal-Symmetry Filter Architectures Using Delta Operator
Oct. 28		Pei-Yu Chen, Lan-Da Van, I. H. Khoo, Hari C. Reddy
Jade Room 2		National Chiao Tung University, Taiwan

SD8 New Devices and Advance Technologies (4)

Session Chair: Francis Balestra, Grenoble INP/CNRS, France

15:45	SD8-1	3D Scaling for Insulated Gate Bipolar Transistors (IGBTs) with Low Vce(sat)
Oct. 28	(Invited)	Kazuo Tsutsui, K. Kakushima, T. Hoshii, A. Nakajima, S. Nishizawa, H. Wakabayashi, I. Muneta, K. Sato, T. Matsudai, W. Saito, T. Saraya, K. Itou, M. Fukui, S. Suzuki, M. Kobayashi, T. Takakura, T. Hiramoto, A. Ogura, Y. Numasawa, I. Omura, H. Ohashi, and H. Iwai
Jade Room 3		Tokyo Institute of Technology, Japan
16:15	SD8-2	World Changing Innovation from Semiconductor Technology
Oct. 28	(Invited)	Ellen Shen
Jade Room 3		Tektronix
16:45	SD8-3	Advanced FinFET Technologies for Boosting SRAM Performance
Oct. 28	(Invited)	Kazuhiko Endo
Jade Room 3		National Institute of Advanced Industrial Science and Technology, Japan
17:15	SD8-4	High-Voltage Bidirectional Current Sensor
Oct. 28	(Invited)	Zong-You Hou, Hsiu-Chun Tsai, Chua-Chin Wang
Jade Room 3		National Sun Yat-Sen University, Taiwan

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