



<http://www.asicon.org>

## First Call for Papers

# IEEE 12<sup>th</sup> International Conference on ASIC

Oct. 25-28, 2017, **Hotel Pullman Guiyang**, Guiyang, China

### General Co-Chairs

**Chenming Hu**  
**Ting-Ao Tang**  
**Jan Van der Spiegel**  
**Richard.M.M.Chen**  
**Satoshi Goto**  
**Yong Lian**

### Advisory Committee Co-Chairs

**Yangyuan Wang**  
**Omar Wing**  
**Qianling Zhang**  
**Hiroshi Iwai**

### Program Committee Co-Chairs

**Zhiliang Hong**  
**Hidetoshi Onodera**  
**Bin Zhao**  
**Yi Zhao**  
**Francois Rivet**

### Organizing Committee Co-Chairs

**Mengqi Zhou**  
**Huihua Yu**  
**Quan Xie**

### Industry Liaison

**Peng Hu**

### Publicity Chair

**Yajie Qin**

### Secretary-General

**Yajie Qin**

*Sponsored by* **IEEE Beijing Section**  
*Co-Sponsored by* **Fudan University**  
*Technical Sponsor* **IEEE CAS Society**  
*Patrons by* **IEEE SSCS Shanghai Chapter**  
**IET Shanghai Network**  
**Chinese Institute of Electronics**  
**Guizhou University**

The 12<sup>th</sup> International Conference on ASIC (ASICON 2017) will be held in Guiyang, China, during Oct. 25-28, 2017. The conference is intended to provide an international forum for VLSI circuit designers, ASIC users, system integrators, IC manufacturers, process and device engineers, and CAD/CAE tool developers to present their latest progress, development and research results in their respective fields. The four-day event features keynote speeches, invited talks, regular paper presentations and tutorials, delivered by leading experts in the respective fields, on state-of-the-art VLSI circuits, design methodology, device, process and manufacturing technologies. The Excellent Student Paper award will be announced at the conference. Additionally, an exhibition on EDA tools, foundry technologies, IC processing/testing facilities, and novel ASIC products will be held during the conference.

### *The Scope of the Conference*

Papers are solicited in, but not limited to, the following:

#### **I. Design Techniques**

- [1] VLSI Design and Circuits
  - Low power techniques, high-speed circuits
  - Embedded processors and DSP
  - Chaos/neural/fuzzy-logic circuits
  - Programmable devices (PLD, EPLD, HDPLD, FPGA, etc)
  - NoC
- [2] Analog, Mixed Signal and RF Circuits
  - Data converters (ADCs and DACs)
  - RF circuits (narrowband RF, ultra low power and millimeter-wave circuits (MMDS, 60GHz), RF/IF and power amplifiers, frequency generators, RF switches, power detectors, active antennas)
  - Power systems and power electronic circuits
- [3] Application-Specific SoCs
  - Automobile electronics and industry control
  - Biomedical circuits and systems
  - Sensory systems
  - Graph theory and computing
  - Neural systems and applications
  - Mobile computing
  - IoT technologies
- [4] Circuits and Systems for Wireless Communications
  - Receiver and transmitter technologies for wireless systems (WLAN, WPAN, WMAN, GPS, DVB/DMB, UWB, Bluetooth, GSM/EDGE/CDMA/UMTS/3G/4G/5G base stations and handsets, TV, radio, satellite)
  - RFID
  - ISM band systems
- [5] Testing, Reliability, Fault-Tolerance
  - Digital/analog/mix-signal testing

- Design for testability and reliability
  - Test vector compression and silicon debug and diagnosis
  - Variation-aware design
  - Static and dynamic defect and fault recoverability
- [6] Advanced Memory
- DRAM & SRAM
  - Flash memory
  - Ferroelectric memory
  - Phase change memory, RRAM, MRAM
- [7] FPGA
- Tools and design technique for FPGA
  - Architectures for FPGA
  - Device technology for FPGA
  - Application of FPGA
- II. CAD Techniques**
- [8] Circuits Simulation, Synthesis, Verification and Physical Design
- Analog circuits modeling and simulation
  - Logic synthesis, simulation and formal verification
  - Partitioning, placement and floor planning
  - Routing and detailed physical design
- [9] CAD for System, Design for Manufacturing and Testing
- Embedded systems
  - Mixed technology/domain, reliable and alternative systems
  - Design for manufacturability and testing
- III. New Techniques, New Processing, New Devices and Their Applications**
- [10] MEMS Techniques
- Piezoelectric and MEMS application
  - Pyroelectric/IR/optical application
  - Sensors, chemical and bio-chips
- [11] Nanoelectronics and Gigascale Systems
- Nano devices and NEMS
- [12] New Devices: Heterojunction Devices, Fin FET, CNT MTJ Devices, 3-D Integration, etc.
- [13] Advanced Interconnection Technology, High-K/Metal Gate Technology and Other VLSL  
New Processing, New Technologies
- [14] VLSI Applications for Energy Generation, Conservation and Control
- [15] Processing Modeling & Simulation
- IV. Other VLSI Design and Device Related Topics**
- [16] Other Devices Related Topics
- [17] Other VLSI Design Related Topics

### ***Papers Submission***

Prospective authors are requested to submit full-length papers in English of no more than four pages using the proceedings format, double columned, 10pt fonts including figures, tables and reference. For further information on the paper format, please refer to "[template](#)". The papers are submitted in their final form and, if accepted, will be published as submitted. All submissions must be made at the conference website. Student authors, who want to compete for the Excellent Student Paper Award, should apply at the conference website. Detailed instructions for paper preparation and submission can be found at conference website. **Tutorial proposals are also invited.**

<b>Contact persons:</b>	<b>Prof. Huihua Yu</b>	<b>Prof. Yajie Qin</b>
	Email: <a href="mailto:asicon_org@fudan.edu.cn">asicon_org@fudan.edu.cn</a>	Email: <a href="mailto:yajieqin@fudan.edu.cn">yajieqin@fudan.edu.cn</a>
	<b>(Conference Issue)</b>	<b>(Paper Submission)</b>

**For further information please visit conference web site:**

**<http://www.asicon.org>**

**Deadline of papers submittal is June 30, 2017**  
**Paper acceptance/rejection will be informed by Aug. 15, 2017**