
The 11th IEEE International Conference on ASIC



www.asicon.org

ASICON 2015

FINAL PROGRAM

Nov. 03-06, 2015

Wangjiang Hotel, Chengdu, China

 **IEEE Beijing Section**

 **復旦大學**
FUDAN UNIVERSITY

 **电子科技大学**
University of Electronic Science and Technology of China

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The 11th International Conference on ASIC

ASICON2015

Nov. 3-6, 2015

Wangjiang Hotel, Chengdu, China

Sponsored by

*IEEE Beijing Section
Fudan University*

Supported by

*University of Electronic Science & Technology of China
Talent Exchange Center,
Ministry of Industry & Information Technology
IEEE SSCS Shanghai Chapter
IET Shanghai Network
Chinese Institute of Electronics (CIE)*

Organized by

Fudan University

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Welcome to ASICON 2015

On behalf of the Conference, it is my great pleasure and honor to express our warm welcome to all ASICON 2015 attendees. Thank you very much for your participation.

ASICON 2015 is the 11th event of this conference series that began in 1994. The Conference will be held from November 3 to 6, 2015 at Wangjiang Hotel, Chengdu, China. Chengdu is a beautiful historical city. We sincerely hope that you will have a rewarding and good time in Chengdu.

While “ASIC” has had a narrow meaning, the Conference has adopted Advanced Semiconductor Integrated Circuits as the meaning of ASIC in ASICON. This normally recognizes the fact that ASICON covers all the technical fields of integrated circuits. The conference provides an international forum for VLSI circuit designers, ASIC users, System Integrators, IC manufacturers and CAD/CAE tool developers to present their new progresses, developments and research results in their respective fields. The Conference also affords a platform for academic and industry attendees to network and exchange information.

ASICON 2015 has invited international experts to give tutorials on the first day of the conference. In addition, we have invited 8 world renowned academic and industry leaders to give keynote speeches on the plenary sessions from Nov. 4-6.

ASICON has a strong positive impact on industry and academia. We look forward to continuing this tradition with you this year.

General Chair of ASICON 2015

Chenming Hu

2015.11

Conference Committee

General Co-Chairs

Name	Affiliation	Country/Area
Chenming Hu	UC Berkeley	USA
Ting-Ao Tang	Fudan University	China
Rakesh Kumar	Technology Connexions, Inc	USA
Richard.M.M. Chen	City University of Hongkong	Hongkong
Satoshi Goto	Waseda University	Japan
Yong Lian	National University of Singapore	Singapore

Advisory Committee Co-Chairs

Yangyuan Wang	Peking University	China
Omar Wing	Columbia University	USA
Ernest Kuh	UC Berkeley	USA
Qianling Zhang	Fudan University	China

Program Committee Co-Chairs

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Linming Jin	Brocade Inc	USA
Hidetoshi Onodera	Kyoto University	Japan
C.K.Cheng	UCSD	USA
Bo Zhang	University of Electronic Science and Technology of China	China

Organizing Committee Co-Chairs

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Huihua Yu	Fudan University	China
Li Ma	MIITEC	China

Industry Liaison		
Peng Hu	CICMAG Com	China
Secretary-General		
Fan Ye	Fudan University	China

Technical Program Committee Members of ASICON 2015

Analog and RF Circuits Subcommittee		
Chen, Junning	Anhui University	China
Chen, Weizen	National Chiao Tung University	Taiwan
Cheng, Jun	Xian Jiaotong University	China
Chi Baoyong	Tsinghua University	China
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Gu, Jane	University of California, Davis	USA
Li, Qiang	University of Electronic Science and Technology of China	China
Lu, Ping	Lund University	Sweden
Sai Weng Sin	University of Macau	Macao
Simon S. Ang	University of Arkansas	USA
Song, Fei	MediaTek Inc	USA
Wu, Nanjian	Institute of Semiconductor, CAS	China
Zhang, Wenjun	Intel Corp.	USA
Zhang, Xiaoyang	National University of Singapore	Singapore
Zhao, Yiqiang	Tianjin University	China
Zhou, Jianjun	Shanghai Jiaotong University	China

Digital Circuits and Systems Subcommittee		
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Chang, Yao-Wen	National Taiwan University	Taiwan
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Gerald E. Sobelman	University of Minnesota	USA

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Jin, Linming	Brocade Communications Systems, Inc.	USA
Jou, Shyh-Jye	National Chiao Tung University	Taiwan
Liu, Liang	Lund University	Sweden
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Wang, Donghui	Institute of Acoustics, CAS	China
Wang, Jinhui	Beijing University of Technology	China
Wang, Zhongfeng	Broadcom Corporation	USA
Wu, An-Yeu	National Taiwan University	Taiwan
Yu, Zhiyi	SYSU-CMU Joint Institute of Engineering	China
Zeng, Xiaoyang	Fudan University	China
Zhou, Dajiang	Waseda University	Japan
Zhang, Tong	Rensselaer Polytechnic Institute	USA

EDA Techniques Subcommittee

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Jerraya, Ahmed	CEA Tech	France
Li, Xiaowei	Institute of Computing Technology, CAS	USA
Sheldon X. D. Tan	University of California, Riverside	China
Shi, Weiping	Texas A & M University	USA
Shi, Youhua	Waseda University	Japan
Wang, Lingli	Fudan University	China
Wang, Pengjun	Ningbo University	China
Wang, Xingang	Skyworks Solutions, Inc.	USA
Wen, Xiaoqing	Kyushu Institute of Technology	Japan
Yu, Hao	Nanyang Technological University	Singapore
Zhou, Hai	Northwestern University	USA

Process and Devices Subcommittee

Hou, Ligang	Beijing University of Technology	China
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Tian-Ling Ren	Tsinghua University	China
Wang, Gaofeng	Hangzhou Dianzi University	China
Yeh, Wen-Kuan	National University of Kaohsiung	Taiwan
Zhang, Naiqian	Dynax Semiconductor Inc.	China
Zou, Xuecheng	Huazhong University of Science and Technology	China

General Information

● Conference Language

The official language is English. No simultaneous translation is available.

● Conference Schedule

Date	Time	Event
Nov. 3 Tue.	AM & PM	Tutorial Session & Registration
Nov. 4 Wed.	AM	Opening & Keynote Session
		Keynote Session (K-1,K-2, K-3,K-4)
	PM	Parallel Sessions
		Parallel Sessions
		Poster Session (1)
	Evening	Reception
Nov. 5 Thur.	AM	Keynote Session (K-5,K-6)
		Parallel Sessions
	PM	Parallel Sessions
		Parallel Sessions
		Poster Session (2)
Nov. 6 Fri.	AM	Keynote Session (K-7,K-8)
		Parallel Sessions
	PM	Parallel Sessions
		Parallel Sessions
	Evening	Banquet

● Conference Site

The conference will be held in **Wangjiang Hotel*******

Tel: +86-28-84090658 Fax: +86-28-84791688

Add: No.42 Xiashahepu Street, Chengdu, Sichuan, P.R.China

Website: www.wangjianghotel.com

● Conference Registration

Payment by Credit Card, Bank Transfer, or Check

1. Participant: Accepted Paper ID Number(if available): _____

Mr. Ms. First Name: _____ Last Name: _____

Affiliation (Univ./Company): _____

Address: _____

Phone: _____ Mobile: _____ Email: _____

2. Registration Fee

Classification	Before Sep.15, 2015	After Sep.15, 2015	Amount
IEEE or IET member*	<input type="checkbox"/> 3500 CNY	<input type="checkbox"/> 3800 CNY	
Non-member	<input type="checkbox"/> 3800 CNY	<input type="checkbox"/> 4100 CNY	
Student	<input type="checkbox"/> 2400 CNY	<input type="checkbox"/> 2700 CNY	
Extra banquet ticket	<input type="checkbox"/> 300 CNY		
Extra pages	<input type="checkbox"/> 400 CNY / page		
Tutorial	<input type="checkbox"/> T-1 & T-2 & T-3 <input type="checkbox"/> T-4 & T-5 & T-6	200 CNY 200 CNY	
<input type="checkbox"/> Vegetarian	<input type="checkbox"/> Need hardcopy Proceedings <input type="checkbox"/> Don't need hardcopy Proceedings	500 CNY	
Total Amount	CNY		

(*IEEE or IETMember)* Member Number: _____

The registration fee covers:

- Admission to all the sessions;
- Three days' meals (Nov.4-6,2015) including the reception (Evening of Nov.4) and the banquet (Evening of Nov.6); Coffee Breaks;
- A conference kit (with a conference bag, a program brochure, and a USB with E-Proceedings).

(The tutorial fee covers the lunch on Nov.3 and tutorial materials. Please visit the conference website for details of the tutorials.)

3. Payment Methods

1) <input type="checkbox"/> Credit Card Date of Payment _____	Please Click Here for Credit Card Payment	_____ CNY
2) <input type="checkbox"/> Bank Transfer Remit date _____ Note: If it is not possible for you to transfer CNY, please transfer USD based on the	Sender's Name _____ Account Name: Fudan University Account Number: 437759252978 Bank Name: 044159 Bank of China Shanghai Guo Ding Road Sub-Branch Bank address: No.288, Guo Ding Rd.. Shanghai, 200433, China	_____ CNY

USD/CNY exchange rate of the day of transfer.	Swift Code: BK CH CN BJ 300 Attn: ASICON 2015	
3) <input type="checkbox"/> Bank Draft/Check Remit date _____	I have enclosed herewith a bank draft/check made payable to Fudan University and sent to Jieting Sheng	_____ CNY

Please send the Registration Form and Payment Receipt to Jieting Sheng by Email or Fax

Email: jtsheng@fudan.edu.cn

Fax: +86-21-65643449

Mailing address: School of Microelectronics, Fudan University,
220 Handan Road, Shanghai, 200433, China

● Registration Desk

The conference registration desk will be located at Chengdu Wangjiang Hotel. The conference registration will be open on Nov. 3 (8: 00~20: 00), Nov. 4~Nov. 6 (8: 00~17: 45). And the registration desk will keep available at the same site throughout the whole conference.

● Transportation

How to get to the Chengdu Wangjiang Hotel:

- Chengdu Shuangliu International Airport is 19.9 km away from hotel, take taxi about 25-min you will arrive at hotel.
- Chengdu Railway Station is 11.6 km away from hotel; it takes you about 20-min walking to the hotel.
- Chengdu Eastern Railway Station is 4.2 km away from hotel; it takes you about 10-min walking to the hotel.

More details about the conference hotel booking, please visit

<http://www.discoverchinatours.com/travel-guide/chengdu-asicon-2015.html>

● Weather

The average temperature during conference time in Chengdu is around 14°C~19°C.

● Visa

All the foreign travelers to China must have a valid visa. Visas may be obtained from the Chinese Embassy or Consulate in most major cities around the world. A conference attendee will be mailed an official invitation letter for visa application after he or she fills and returns the Visa Application Form (<http://www.asicon.org>) to asicon_org@fudan.edu.cn timely.

● Awards

Excellent Student Paper Awards will be announced at the banquet on Nov. 6. To be qualified for the Excellent Student Paper Award, the paper must be presented by the student himself or herself (1st author). The Technical Program Committee and Organizing Committee will choose through public appraisal some excellent student papers from the candidates.

Paper Presentation Information

The ASICON2015 will have oral and poster sessions. All the papers included in the conference program should be presented in English by one of the authors at the arranged sessions.

● Oral Presentation

Presentation time:

Invited paper (20~30 minutes): 15~25 min talk + 5 min Q/A

Regular paper (12~15 minutes): 10~12 min talk + 2~3 min Q/A

Computer and digital projector will be provided in each meeting room.

● Poster Presentation

Poster size: 120 cm (high) × 100 cm (wide)

Poster Session 1:

Setup time: 8: 30-17: 30 on Nov. 4

Presentation time: 17: 45-18: 45 on Nov. 4 (on the spot)

Display time: 8: 30-21: 00 on Nov. 4

Poster Session 2:

Setup time: 8: 30-17: 30 on Nov. 5

Presentation time: 17: 45-18: 45 on Nov. 5 (on the spot)

Display time: 8: 30-21: 00 on Nov. 5

Thumb pins, adhesive tapes, and scissors will be provided at the registration desk. The poster should be taken off by 21: 30 by the author if he or she would like to keep it. After that time, it will be removed and be regarded as being discarded by the authors.

● Coffee Break

Complementary coffee/tea will be served in each morning/afternoon session. The break will take place in general at 10: 00-10: 15 during morning sessions and 15: 30-15: 45 during afternoon sessions. Due to time schedule of different sessions, the actual break time may have slight variation. Coffee/tea will be served in about half-hour duration.

● Meeting Room Location

Meeting Room	Location
Maesai Reception Hall	Wangjiang Club 1 rd Floor
Brunei Meeting Room	Wangjiang Club 2 nd Floor
Penang Island Meeting Room	Wangjiang Club 2 nd Floor
Penang Meeting Room	Wangjiang Club 2 nd Floor
Wufu Hall	Wufu Building 1 rd Floor

Tutorial Session

Tuesday, November 3, 8: 30 – 12: 15

Tuesday, November 3, 8: 30 – 12: 15
Tutorial Session T-1 & T-2

Maesai Reception Hall
Wangjiang Club 1F

- T-1 New and Effective Methodologies for System-Level Electrostatic Discharge (ESD Characterization) (8: 30-10: 00)**
Prof. Juin J. Liou, University of Central Florida, USA
- T-2 Fundamentals of Bulk FinFETs (10: 15-12: 15)**
Prof. Jong-Ho Lee, Seoul National University, Korea

Tuesday, November 3, 8: 30 – 12: 15
Tutorial Session T-4 & T-5

Brunei Meeting Room
Wangjiang Club 2F

- T-4 Improving DC-DC Converter Performance with GaN Transistors (8: 30-10: 00)**
Dr. Alex Lidow, CEO of Efficient Power Conversion Corporation

- T-5 New Challenges and Techniques for Clock Domain Crossing and Reset Sign-off (10: 15-12: 15)**
Mr.Ramesh Dewangan, VP of Product Strategy in Real Intent, USA

Tuesday, November 3, 13: 30 – 16: 30

Tuesday, November 3, 13: 30 – 16: 30
Tutorial Session T-3

Maesai Reception Hall
Wangjiang Club 1F

- T-3 Ultra-Low Power Digital Design Approaches for the Internet of Things (13: 30-16: 30)**
Prof. Massimo Alioto, National University of Singapore, Singapore

Tuesday, November 3, 13: 30 – 16: 30
Tutorial Session T-6

Brunei Meeting Room
Wangjiang Club 2F

- T-6 CMOS Operational Amplifiers Design (13: 30-16: 30)**
Dr. Zhongyuan Chang, Montage technology, China

Technical Session

Wednesday

Wednesday, November 4, 8: 30 – 10: 30

Wednesday, November 4, 8: 30 –10: 30

Wufu Hall

Opening & Keynote Session K-1 & K-2

Wangjiang Hotel 1F

K-1 Modern circuit techniques for wireless communication (9: 00-9: 45)

Prof. Bram Nauta (Twente University, Netherland)

K-2 The Evolution of Memory Solutions for New IT era and its Challenges (9: 45-10: 30)

Mr. Jonghoon Oh, Corp VP and GM of DRAM (Product Development Div, SK Hynix, Korea)

Wednesday, November 4, 10: 45– 12: 15

Wednesday, November 4, 10: 45–12: 15

Wufu Hall

Keynote Session K-3 & K-4

Wangjiang Hotel 1F

K-3 The Impact of IoT from Silicon to Software (10: 45-11: 30)

Dave De Maria, VP Corporate Marketing (Synopsys, USA)

K-4 FinFETs: From Devices to Architectures (11: 30-12: 15)

Prof. Niraj K Jha, IEEE Fellow, ACM Fellow (Princeton University, USA)

Wednesday, November 4, 13: 30 – 15: 30

Wednesday, November 4, 13: 30 – 15: 30	Maesai Reception Hall Wangjiang Club 1F
Session A1 : Image & Sound Processing	
Session Chair : Gensheng Chen, <i>Fudan University</i>	

	Title
A1-1	0433: CMOS Image Sensor with Programmable Compressed Sensing
13: 30	Huixian Ye, Li Tian, Qi Zhang, Hui Wang, Songlin Feng (<i>Shanghai Advanced Research Institute, Chinese Academy of Sciences</i>)
A1-2	0451: High-speed object detection based on a hierarchical parallel vision chip
13: 45	Zhongxing Zhang, Jie Yang, Honglong Li, Liyuan Liu, Jian Liu, Nanjian Wu (<i>State Key Laboratory for Superlattices and Microstructures, Institute of Semiconductors Chinese Academy of Sciences, Beijing</i>)
A1-3	0470: Implementation of High Performance Hardware Architecture of Face Recognition Algorithm Based on Local Binary Pattern on FPGA
14: 00	Yangjie Zhang, Wei Cao, Lingli Wang (<i>State Key Laboratory of ASIC and System, Fudan University, Shanghai</i>)
A1-4	0572: A Novel Vision Chip Architecture for Image Recognition Based on Convolutional Neural Network
14: 15	Honglong Li, Zhongxing Zhang, Jie Yang, Liyuan Liu, Nanjian Wu (<i>State Key Laboratory for Superlattices and Microstructures, Institute of Semiconductors Chinese Academy of Sciences, Beijing</i>)
A1-5	0723: The Design of Face Recognition System Based on ARM9 Embedded Platform
14: 30	Feng Ru, Xiaohong Peng, Ligang Hou, Jinhui Wang, Shuqin Geng, Chen Song (<i>VLSI and System Lab, Beijing University of Technology</i>)
A1-6	0563: Iterative optimization algorithm for sound localization
14: 45	Fang Sun, Jin-mei Lai (<i>State Key Laboratory of ASIC and System, Fudan University, Shanghai</i>)

Wednesday, November 4, 13: 30 – 15: 30	Brunei Meeting Room Wangjiang Club 2F
Session B1 : Digital Module	
Session Chair : Yajuan He, <i>University of Electronic science and Technology of China</i>	

	Title
B1-1	0413: Opportunities and Challenges: Ultra-Low Voltage Digital IC Design Techniques (invited paper)
13: 30	Tony Kim (<i>Nanyang Technological University, Singapore</i>), Jun Zhou (<i>Institute of Microelectronics, A*STAR, Singapore</i>), Yong Lian (<i>National University of Singapore</i> ,

	<i>Singapore)</i>
B1-2	0749: Nanoscale Register File Circuit Design –Challenges and Opportunities (invited paper)
14: 00	Khawar Sarfraz, Mansun Chan (<i>Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology</i>)
B1-3	0427: A Quenching-and-Reset Circuit with Programmable Hold-off Time for Single Photon Avalanche Diodes in 0.18-μm CMOS
14: 30	Jinglin Huang, Qi Zhang, Li Tian, Hui Wang, and Songlin Feng (<i>School of Information and Technology, Shanghai Tech University, Shanghai, China, Shanghai Advanced Research Institute, Chinese Academy of science, Shanghai, China</i>)
B1-4	0649: A 0.3V-to-1.1V Standard Cell Library in 40nm CMOS
14: 45	Jintao Li, Hong Chen, Zhihua Wang (<i>Institute of Microelectronics, Tsinghua University, Beijing, China</i>), Ming Liu (<i>Institute of Semiconductors, Chinese Academy of Sciences, Beijing, China</i>)
B1-5	0506: A low-power soft error tolerant latch scheme
15: 00	Saki Tajima, Youhua Shi, Nozomu Togawa, Masao Yanagisawa (<i>Waseda University, Okubo, Japan</i>)
B1-6	0544: Energy-efficient Sub-threshold Level Shifter
15: 15	Liang Wen, Li Li, Haibo Wen, Xiaoyang Zeng (<i>State-Key Lab of ASIC and System, Fudan University, Shanghai</i>)
B1-7	0353: A Low Voltage SRAM Sense Amplifier with Offset Cancelling Using Digitized Multiple Body Biasing
15: 30	Bingyan Liu, Yong Hei (<i>ASIC & System Department, Institute of Microelectronics Chinese Academy of Sciences</i>)

Wednesday, November 4, 13: 30 – 15: 30	Penang Island Meeting Room
Session C1 : RF Circuit 1	Wangjiang Club 2F
Session Chair : Yumei Huang, <i>Fudan University</i>	

	Title
C1-1	0392: 2.4/5.5GHz LNA Switch Designs Based on High Resistive Substrate 0.35um SiGe BiCMOS (invited paper)
13: 30	Chaojiang Li, Vibhor Jain, Hanyi Ding, Myra Boenke, Dawn Wang, Randy Wolf, Alvin Joseph (<i>GlobalFoundries, Vermont, USA</i>), Xiaoxia Wang (<i>GlobalFoundries, Shanghai, China</i>)
C1-2	0512: Toward 5G: an Integrated CMOS Wide Band Arbitrary Waveform Generator for Carrier Aggregation (invited paper)
13:58	Yann Deval, Yoan Veyrac, Francois Rivet (<i>IMS Laboratory, University of Bordeaux</i> ,

	<i>Talence, France)</i>
C1-3	0570: A 57 to 66 GHz Novel Six-Port Correlator (invited paper)
14: 26	Peng Siew Chew, Zhi Hui Kong (<i>School of Electrical Engineering, Nanyang Technological University, Singapore</i>) Kiat Seng Yeo (<i>Singapore University of Technology and Design(SUTD),Singapore</i>) Kaixue MA (<i>University of Electronic science and Technology of China (UESTC), Chengdu,China</i>)
C1-4	0688: A Multi-mode Reconfigurable Lowpass/Complex Bandpass CT $\Sigma \Delta$ Modulator for Short Range Wireless Receiver
14: 54	Guodong Zhu, Junfeng Zhang, Yang Xu, Zehong Zhang, Baoyong Chi (<i>Institute of Microelectronics, Tsinghua University, Beijing, China</i>)
C1-5	0597: A 100M-1.5 GHz Harmonic-Rejection SDR Receiver Front-End
15: 06	Feng Ma, Xin-Wang Zhang, Bao-Yong Chi (<i>Institute of Microelectronics, Tsinghua University, Beijing, China</i>)
C1-6	0593: A SFA and I/Q Mismatch Auto-calibration Scheme For High IRR Multi-mode GPS RF Receiver
15: 18	Qin Chen, Dongpo Chen, Tingting Mo (<i>School of Microelectronics, Shanghai Jiao Tong University, China</i>)

Wednesday, November 4, 13: 30 – 15: 30	Penang Meeting Room
Session D1 : Power Management	Wangjiang Club 2F
Session Chair : Ping Luo, <i>University of Electronic science and Technology of China</i>	

	Title
D1-1	0786: An Input-Powered 1.1-μA IQ 13.56 MHz RF Energy Harvesting System for Biomedical Implantable Devices (invited paper)
13: 30	James Davis, Joseph Sankman, Dongsheng Ma (<i>Integrated System Design Laboratory Texas Analog Center of Excellence (TxACE) The University of Texas</i>)
D1-2	0497: High Efficiency Single-Inductor Dual-Output DC-DC Converter with ZVS-PWM Control
14: 00	Yoshiki Sunaga, Naoya Shiraishi, Koyo Asaishi, Nobukazu Tsukiji, Yasunori Kobori, Nobukazu Takai, Haruo Kobayashi (<i>Division of Electronics and Informatics, Graduate School of Science and Technology, Gunma University, Japan</i>)
D1-3	0729: A 3.5-A Buck DC-DC Regulator with Wire Drop Compensation for Remote-Loading Applications
14: 15	Lei Zhu, Qi Cheng, Jianghui Deng, Xidong Ding (<i>School of Physics and Engineering, Sun Yat-sen University, Guangzhou, China</i>), Jianping Guo, Dihu Chen (<i>School of Microelectronics, Sun Yat-sen University, Guangzhou, China; SYSU-CMU Shunde International Joint Research Institute, Foshan, China</i>)

D1-4	0453: A Distributive On-Chip Voltage Regulation Scheme for Power Supply Design in AMOLED Driver ICs
14: 40	Weikai Jiang, Hing-Mo Lam, Hesheng Lin, Min Zhang (<i>School of Electronic and Computer Engineering, Peking University, Shenzhen, China</i>), Hui Shao (<i>Shenzhen Chipsvision Micro Co. Ltd., Shenzhen, China</i>)
D1-5	0545: A Load-transient-Enhanced Output-Capacitor-Free Low-Dropout Regulator Based on an Ultra-Fast Push-Pull Amplifier
14: 45	Shaowei Zhen, Ji Wang, Dongjie Yang, Canhua Cao, Ping Luo (<i>State Key Laboratory of Electronic Thin Films and Integrated Devices; University of Electronic Science and Technology of China, Chengdu, 610054, China</i>)
D1-6	0552: Low Dropout Voltage Regulator with Ultra Fast Sensing Feedback Mechanism
15: 00	Hareharan Nagarajan, Kaushik Saha , Subash PM, Sumit Johar (<i>Visual Display- SoC, Samsung R & D Institute India Ltd., India</i>)
D1-7	0326: An Adaptive Voltage Scaling Circuit Based on Dominate Pole Compensation
15: 15	Ping Luo, Songlin Fu, Xiang Zhang, Yi Bao, Dongjun Wang (<i>State Key Laboratory of Electronic Thin Films and Integrated Devices University of Electronic Science and Technology of China, Chengdu, China</i>)

Wednesday, November 4, 15: 45-17: 45

Wednesday, November 4, 15: 45-17: 45	Maesai Reception Hall
Special Session : Advanced ESD Protection Designs for ICs	Wangjiang Club 1F
Session Chair : He Tang, <i>University of Electronic science and Technology of China</i>	

	Title
A2-1	0464: Development of High-Voltage ESD Protection Devices on Smart Power Technologies for Automotive Applications (invited paper)
15: 45	Carol(Rouying) Zhan, Changsoo Hong (<i>Freescale Semiconductor, USA</i>), Jean-Philippe Laine, Patrice Besse (<i>Freescale Semiconductor, France</i>)
A2-2	0465: TLP Evaluation of ESD Protection Capability of Graphene Micro-Ribbons for ICs (invited paper)
16: 15	Wei Zhang, Ming Xia, Ya-Hong Xie (<i>Department of Materials Science and Engineering, University of California, Los Angeles</i>), Qi Chen, Rui Ma, Fei Lu, Chenkun Wang, Albert Wang (<i>Department of Electrical Engineering, University of California, Riverside</i>)
A2-3	0565: Function-Based ESD Protection Circuit Design Verification for BGA Pad-Ring Array (invited paper)

16: 45	Li Wang (<i>Skyworks Solutions, USA</i>), Rui Ma, Fei Lu, Albert Wang (<i>Dept. of ECE, University of California, Riverside</i>), Zongyu Dong (<i>Qualcomm, USA</i>), Xin Wang (<i>OmniVision Technologies, USA</i>), Chen Zhang, Bin Zhao, Siqiang Fan (<i>Fairchild, USA</i>), He Tang (<i>UESTC, China</i>)
A2-4	0624: Compact Modeling of Junction Failure in Semiconductor Devices Subject to Electrostatic Discharge Stresses (invited paper)
17: 15	Juin J. Liou (<i>University of Central Florida</i>), Zhiwei Liu (<i>University of Electronic Science and Technology China</i>)

Wednesday, November 4, 15: 45-17: 45	Brunei Meeting Room
Session B2 : System-Level Design Methodology	Wangjiang Club 2F
Session Chair : Goro Suzuki, <i>University of Kitakyushu</i>	

	Title
B2-1	0340: Waveform Base Clock Tree Delay Analysis Using Parallel Processing (invited paper)
15: 45	Goro Suzuki (<i>University of Kitakyushu, Japan</i>)
B2-2	0438: Optimal design on Asynchronous System with Gate-level pipelining
16: 15	Masato Tamura, Atsushi Ito, Makoto Ikeda (<i>Department of Electrical Engineering and Information System, The University of Tokyo, Japan</i>)
B2-3	0626: Clock Skew Estimate Modeling for FPGA High-level Synthesis and Its Application
16: 30	Koichi Fujiwara, Kazushi Kawamura, Masao Yanagisawa, Nozomu Togawa (<i>Department of Computer Science and Communication Engineering, Waseda University</i>)
B2-4	0474: Transaction Level Model of HDMI Transmitter Based on System Verilog
16: 45	Xiang Liang, Ligang Hou, Jinhui Wang, Chunhui Yang, Deyang Gao, Lin Zhu (<i>VLSI and System Lab, Beijing University of Technology, China</i>)
B2-5	0423: A Novel Low-cost Interface Design for systemc and systemverilog co-simulation
17: 00	Yunzhong Zhu, Tao Li, Jingpeng Guo, Fangfa Fu (<i>Microelectronics Center, Harbin Institute of Technology, Harbin, China</i>), Haiyang Zhou (<i>Beijing Microelectronics Technology Institute, Beijing, China</i>)
B2-6	0322: Simultaneous Scheduling and Binding for Resource Usage and Interconnect Complexity Reduction in High-Level Synthesis
17: 15	Cong Hao, Jian-Mo Ni, Hui-Tong Wang, Takeshi Yoshimura (<i>Graduate School of IPS, Waseda University, Japan</i>)

B2-7	0358: Primal-Dual Method based Simultaneous Functional Unit and Register Binding
17: 30	Jianmo Ni, Qian Ai(<i>Dept. of Electrical Engineering, Shanghai Jiao Tong University, Shanghai, China</i>), Cong Hao, Takeshi Yoshimura(<i>Graduate School of IPS, Waseda University, Kitakyusyu, Japan</i>), Nan Wang(<i>School of Information Science and Engineering, East China University of Science and Technology, Shanghai, China</i>)

Wednesday, November 4, 15: 45-17: 45	Penang Island Meeting Room Wangjiang Club 2F
Session C2 : Other ADC & DAC Module	
Session Chair : Fan Ye, Fudan University	

	Title
C2-1	0800: Event-Driven Analog-to-Digital Converter for Ultra Low Power Wearable Wireless Biomedical Sensors (Invited paper)
15: 45	Zhenzhen Tian, Rendong Ying, Peilin Liu, Guoxing Wang, Yong Lian(<i>School of Microelectronics and Electronic Information and Electrical Engineering Shanghai Jiao Tong University</i>)
C2-2	0406: A 14b 1GS/s DAC with SFDR > 80 dBc Across the Whole Nyquist Band by Mixed Total 3-Dimesional Sort-and-Combine and Dynamic Element Matching
16: 15	Shuo Huang, Xuan Li, Xiaoyong Li(<i>Center for Analog/RF Integrated Circuit, School of Microelectronics, Shanghai Jiao Tong University</i>)
C2-3	0514: A 14-bit 2-GS/s DAC with a Programmable Interpolation Filter
16: 30	Feng Ye, Haijun Wang, Ting Yi, Zhiliang Hong(<i>State Key Laboratory of ASIC & System, Fudan University</i>)
C2-4	0366: Finite Aperture Time Effects in Sampling Circuit
16: 45	Miho Arai, Isao Shimizu, Haruo Kobayashi, Keita Kurihara, Shu Sasaki, Shohei Shibuya(<i>Gunma University</i>), Kiichi Niitsu(<i>Nagoya University</i>), Kazuyoshi Kubo(<i>Oyama National College of Technology</i>)
C2-5	0370: Noise Analysis of a CDS with offset cancelling
17: 00	Xiao Wang(<i>Shenyang Institute of Automation, Chinese Academy of Sciences, University of the Chinese Academy of Sciences, Key Laboratory of Opto-Electronic Information Processing, Chinese Academy of Sciences</i>), Zelin Shi, Baoshu Xu(<i>Shenyang Institute of Automation, Chinese Academy of Sciences, Key Laboratory of Opto-Electronic Information Processing, Chinese Academy of Sciences</i>)
C2-6	0301: An Improved voltage Bandgap Reference With high-order curvature compensation
17: 15	Nan Lyu, NingMei Yu, Min Yi(<i>Xi'an University of Technology</i>)

C2-7	0391: A 30 nA, 6.6 ppm/$^{\circ}$C, high PSRR subthreshold CMOS voltage reference
17: 30	Yongquan Li, Mei Jiang, Liangwei Cai(<i>College of Information Engineering, Shenzhen University</i>)

Wednesday, November 4, 15: 45-17: 45	Penang Meeting Room Wangjiang Club 2F
Session D2 : Wireline Communication Session Chair : Gensheng Chen, Fudan University	

	Title
D2-1	0452: Circuit Design Techniques for Multimedia Wireline Communications (invited paper)
15: 45	Chulwoo Kim(<i>Department of Electrical Engineering, Korea University</i>)
D2-2	0579: Low Noise Coupling Techniques for Multi-Phase Oscillators (invited paper)
16: 15	Fa Foster Dai, Feng Zhao, Rong Jiang (<i>Department of Electrical and Computer Eng., Auburn University</i>)
D2-3	0377: LVDS Transmitter With Optimized High Power-efficiency 8: 1 MUX
16: 45	Yuan Su, Yimin Wu, Qiang Zhang, Xuerong Zhou, Fan Ye, Junyan Ren(<i>State Key Laboratory of ASIC & System Department of Microelectronics, Fudan University</i>)
D2-4	0387: Influence of Substrate Coupling Noise to Clock and Data Recovery
17: 00	Yongsheng Wang, Min Wang, Huaixin Xian, Yunfei Du, Xiaowei Liu(<i>Micro-electronic department, Harbin Institute of Technology</i>), Bei Cao(<i>Electronic Science and technology Post-Doctoral Research Center, Heilongjiang University</i>)
D2-5	0663: A 50Gb/s Low Power PAM4 Transmitter with 4-tap FFE and High Linearity Output Voltage in 65nm CMOS Technology
17: 15	Fangxu Lv(<i>Tsinghua National Laboratory for Information Science and Technology, Institute of Microelectronics Tsinghua University, Air and Missile Defense College, Air Force Engineering University</i>), Xuqiang Zheng, Ziqiang Wang, Fule Li(<i>Tsinghua National Laboratory for Information Science and Technology, Institute of Microelectronics Tsinghua University</i>), Jianye Wang(<i>Air and Missile Defense College, Air Force Engineering University</i>)
D2-6	0606: A Power Efficient Current-Mode Differential Driver for FPGAs
17: 30	Yuanlong Xiao, Jian Wang, Jinmei Lai(<i>State Key Laboratory of ASIC and System, Fudan University</i>)

Wednesday, November 4, 17: 45 – 18: 45		
Wednesday, November 4, 17: 45 – 18: 45 Post Session (I)	Wufu Hall Wufu building 1F	

	Title
P1-01	0375: A DPA Resistant Dual Rail Precharge Logic Cell
	Xiao Pang, Jing Wang, Chenxu Wang, Xinsheng Wang(<i>Microelectronics Center, Harbin Institute of Technology at Weihai</i>)
P1-02	0390: A Method of Automatic Sizing Logic Driver of 16nm Fin-FET
	ZengFa Peng, JianBin Zheng, AiLin Zhang(<i>Spreadtrum Co. Ltd.</i>)
P1-03	0407: Design of Power-up and Arbiter Hybrid Physical Unclonable Functions in 65nm CMOS
	Yuejun Zhang, Pengjun Wang, Gang Li, Haoyu Qian, Xiaomin Zheng(<i>Institute of Circuits and Systems, Ningbo University</i>)
P1-04	0486: Development of TFET 0.13 μm Standard Cell Library for Ultra-Low Power Applications
	Fang Gao, Jipan Huang, Hongying Chen, Xin'an Wang(<i>The Key Laboratory of Integrated Microsystems, School of ECE, Peking University Shenzhen Graduate School</i>)
P1-05	0620: Design on Multi-bit Adder Using Sense Amplifier-Based Pass Transistor Logic for Near-Threshold Voltage Operation
	Fangyuan Dang(<i>Shenzhen Graduate School, Peking University, Institute of Microelectronics, Peking University</i>), Yuan Wang, Yuequan Liu, Song Jia, Xing Zhang(<i>Institute of Microelectronics, Peking University</i>)
P1-06	0743: A New Schmitt Trigger with Adjustable Hysteresis Using Floating-Gate MOS Threshold Inverter
	Guoqiang Hang(<i>School of Information and Electrical Engineering, Zhejiang University City College, State Key Laboratory of ASIC & System, Fudan University</i>), Guoquan Li(<i>School of Information and Electrical Engineering, Zhejiang University City College, Institute of Information and Communication Engineering, Zhejiang University</i>)
P1-07	0754: PDK Design of 0.13um SOI PROCESS
	Jiang Bingjian, Junli sheng, Zhangwen Tang(<i>ASIC & System State Key Laboratory, Fudan University</i>)
P1-08	0006: Comparison of Decoupling Resistors and Capacitors for Increasing the Single Event Upset Resistance of SRAM Cells
	Zhongshan Zheng, Zhentao Li, Ning Qiao, Kai Zhao, Fang Yu, Jiajun Luo(<i>Institute of Microelectronics, Chinese Academy of Sciences</i>)
P1-09	0314: A NanoPower, High PSRR Full CMOS Voltage Reference Circuit

	Consisting of Subthreshold MOSFETs
	Jian Li, Jiancheng Li(<i>School of Electronic Science and Engineering, National University of Defense Technology</i>), Li Yang(<i>School of Physics and Optoelectronics Engineering, Xiangtan University</i>)
P1-10	0330: A 1-V 2.5-ppm/$^{\circ}\text{C}$ Second-order Compensated Bandgap Reference
	Meilin Wan, Kui Dai, Xuecheng Zou(<i>School of Optical and Electronic Information, Huazhong University of Science and Technology</i>), Zhenzhen Zhang(<i>Tonghao Department, Wuhan Metro Group Co. Ltd.</i>)
P1-11	0337: An Analytical Series Resistance Model for On-Chip Stacked Inductors with Inclusion of Proximity Effect Between stacked layers
	Wanghui Zou, Yun Zeng(<i>School of Physics and Microelectronics, Hunan University</i>)
P1-12	0351: A High Reliability Synchronous Boost Converter with spike suppression circuit
	Jiangping He, Bo Zhang(<i>Department of Microelectronics, University of Electronic Science and Technology of China</i>), Pengfei Liao(<i>Analog IC Design Department, Chongqing Acoustoelectric and Optoelectronic Co.</i>)
P1-13	0399: A Low Cost Readout and Processing Circuit for Integrated CMOS Geomagnetic Sensors
	Ke Liu, Renwei Zhang, Zhankun Du, Li Shao, Xiao Ma(<i>Institute of Microelectronics, Chinese Academy of Sciences</i>)
P1-14	0435: Dual Band Power Amplifier for Handset Application
	Jie Jin, Xiaoxiao Jiang, Yiyuan Fang(<i>Shanghai University of Engineering Science</i>), Xuguang Zhang(<i>RDA Microelectronic Corporation</i>)
P1-15	0436: Color Image Enhancement Using Power-constraint Histogram Equalization for AMOLED
	Hu Cao, Li Tian, Jun Liu, Hui Wang, Songlin Feng(<i>Shanghai Advanced Research Institute, Chinese Academy of Sciences</i>)
P1-16	0469: Investigation on the Immunity of Microcontroller to Electrical Fast Transients
	Chuangwei Li, Jiancheng Li, Jianfei Wu, Yu Xiao(<i>College of Electronic and Engineering, National University of Defense Technology</i>)
P1-17	0473: A 16-Channel Electrode Driver with Precise calibration for Electrical Neural Stimulation
	Chao Peng (<i>Department of Information Science and Technology, University of Science and Technology of China, Institute of Biomedical and Health Engineering, Shenzhen Institutes of Advanced Technology, Chinese Academy of Sciences</i>), Jinyong Zhang, Lei

	Wang(<i>Institute of Biomedical and Health Engineering, Shenzhen Institutes of Advanced Technology, Chinese Academy of Sciences</i>), Xu Zhang(<i>Department of Information Science and Technology, University of Science and Technology of China</i>)
P1-18	0496: Design and Implementation of Light Load Energy Saving Current-limiting Circuit
	Tao Zhang, Jiyao Zhang (<i>Department of Information Science, Wuhan University of Science and Technology</i>)
P1-19	0503: A 1.2-V 7.2-μw ECG AFE With Continuous Time Self-Calibration Filters
	Feng Huang, Ke Lin, Fang Gao, Chen Chen, Haibin Shao, Bo Wang(<i>The Key Lab of IMS, School of ECE, Peking University Shenzhen Graduate School</i>)
P1-20	0553: Ultra Low Power Circuits Design based on III-V Group Heterojunction Tunnel Field Effect Transistor
	Jipan Huang, Fang Gao, Xin'an Wang, Hongying Chen(<i>The Key Laboratory of Integrated Micro-systems Science and Engineering Applications, Peking University Shenzhen Graduate School</i>)
P1-21	0573: Design of the 1.0V Bandgap Reference on Chip
	Hui Shi, Zheng Sun, Yong Xu, Wei Ding(<i>College of Communication Engineering, PLA University of Science and Technology</i>), Cheng Hu(<i>College of Science, PLA University of Science and Technology</i>), Shan Luo(<i>College of Defense Engineering, PLA University of Science and Technology</i>)
P1-22	0590: A Low-Power Parallel-to-Serial Conversion Circuit for CMOS Image Sensors
	Jicun Zhang, Nan Chen, Chuanming Liu, Libin Yao(<i>Kunming Institute of Physics</i>)
P1-23	0602: A Fully Integrated 0.18 μm SiGe BiCMOS Power Amplifier
	Guojun Liu(<i>Shanghai Huahong Grace Semiconductor Manufacturing Corporation</i>)
P1-24	0653: A Novel Oscillator-Based TRNG for Smart IC Card
	Xiaoyan Jia, Liji Wu, Beibei Wang, Xiangmin Zhang(<i>Tsinghua National Laboratory for Information Science and Technology Institute of Microelectronics, Tsinghua University</i>)
P1-25	0669: A 20μW Dual-Channel Analog Front-End in 65nm CMOS for Portable ECG Monitoring System
	Shuo Li, Nan Qi, Zhiliang Hong (<i>State Key Laboratory of ASIC & System, Fudan University</i>), Vahid Behravan(<i>School of EECS, Oregon State University</i>), Patrick Y. Chiang(<i>State Key Laboratory of ASIC & System, Fudan University, School of EECS, Oregon State University</i>)

P1-26	0700: Low Noise Design of 32-channel snapshot X-ray Readout IC
	Dan Liu, Feng Gao, Liguang Hao(<i>The First Research Institute of Ministry of Public Security</i>)
P1-27	0704: Design of A Novel High-accuracy LED Driving Chip
	Guangfa Si, Yongsheng Yin, Honghui Deng(<i>Institute of VLSI design, Hefei University of Technology</i>)
P1-28	0750: A High PSR SOI Current-mode Bandgap Reference
	Junli Sheng, Bingjian Jiang, Zhangwen Tang(<i>ASIC & System State Key Laboratory, Fudan University</i>)
P1-29	0758: An Overview of Soft-Switching Technique for Flyback Converters
	Xiaofei Chen, Xiaorui Liu, Yingjie Zhang, XueCheng Zou(<i>School of Optical and Electronic Information, Huazhong University of Science and Technology</i>), Shuangxi Lin(<i>School of Electrical and Information Engineering, Wuhan Institute of Technology</i>)
P1-30	0779: A Hall Sensor Microsystem for Current Measurement Used in Watt-hour Meter
	Wenhao Xu, Xunhua Guo, Guoxing Wang(<i>School of Microelectronics, Shanghai Jiao Tong University</i>), Jinling Chen(<i>Wasion Group Limited</i>)
P1-31	0317: An Area-Efficient 10-bit Two-Stage DAC for Active Matrix Organic Light-Emitting Diodes Display Drivers
	Zunkai Huang, Yiling Ding, Li Tian, Qi Zhang, Hui Wang, Songlin Feng (<i>Shanghai Advanced Research Institute, Chinese Academy of Sciences</i>)
P1-32	0373: Energy-efficient and area-efficient switching scheme for SAR ADCs
	Dongsheng Liu, Weila Lei, Yin Liu, Lun Li (<i>School of Optical and Electronic Information, Huazhong University of Science & Technology</i>)
P1-33	0412: A 6b 2b/cycle SAR ADC beyond 1GS/s with Hybrid DAC Structure and Low Kickback Noise Comparators
	Long Zhao, Chenxi Deng, Yuhua Cheng(<i>Shanghai Research Institute of Microelectronics, Peking University, College of EECS, Peking University</i>)
P1-34	0457: A 6bit 4GS/s Current-steering Digital-to-Analog Converter in 40nm CMOS with Adjustable Bias and DfT Block
	Long Zhao, Yuhua Cheng (<i>Shanghai Research Institute of Microelectronics, Peking University, College of EECS, Peking University</i>), Ji He(<i>Shanghai Research Institute of Microelectronics, Peking University</i>)
P1-35	0578: Research of Segmented 8bit Voltage-Mode R-2R Ladder DAC
	Wei Xu, Runxi Zhang(<i>Institute of Microelectronics Circuit & System, East China</i>)

	<i>Normal University), Chunqi Shi(Institute of Microelectronics Circuit & System, East China Normal University, Shanghai Key Laboratory of Multidimensional Information Processing)</i>
P1-36	0598: A 20MHz BW 35fJ/conv. Continuous-Time $\Sigma\Delta$ Modulator with Single-Opamp Resonator Using Finite GBW Compensation Method
	<i>Zemin Feng, Jingjing Wang, Chixiao Chen, Jun Xu, Junyan Ren(State Key Laboratory of ASIC and Systems, Fudan University)</i>
P1-37	0607: 100MS/s 9-bit 0.43mW SAR ADC with Custom Capacitor Array
	<i>Jingjing Wang, Rongjin Xu, Chixiao Chen, Fan Ye, Jun Xu, Junyan Ren(State-key Laboratory of ASIC and system, Fudan University)</i>
P1-38	0618: Adaptive Semiblind Background Calibration of Timing Mismatches in an M-Channel Time-Interleaved Analog-to-Digital Converter
	<i>Sujuan Liu, Haixiao Ma, Jiashuai Cui(School of Electronic Information and Control Engineering, Beijing University of Technology)</i>
P1-39	0769: A 0.4V 53dB SNDR 250 MS/s Time-Based CT $\Delta\Sigma$ Analog to Digital Converter
	<i>Hung-Kai Chen, Wei-Zen Chen(Institute of Electronics, National Chiao Tung University), Zhiyuan Ren(School of Telecommunications Engineering, Xidian University)</i>
P1-40	0784: A Calibration Technique for SAR ADC Based on Code Density Tes
	<i>Xian Gu, Xiuju He, Fule Li(Institute of Microelectronics, Tsinghua University)</i>
P1-41	0792: A 10-bit DAC with 2.9-μV Low Frequency Noise for High Performance MEMS Capacitive Accelerometer Application
	<i>Quan Sun, Min Qi, Yi Gu, Liang Tang, Donghai Qiao(Institute of Acoustics, Chinese Academy of Science)</i>
P1-42	0321: A 125KHz Low Frequency Power Recovery Circuit for Battery-less TPMS SoC
	<i>Yi Wang, Liji Wu, Zhiyuan Tu, Xiangmin Zhang (Tsinghua National Laboratoryfor Information Science and Technology Institute of Microelectronics, Tsinghua University), Wen Jia(Research Institute of Tsinghua University in Shenzhen)</i>
P1-43	0357: A Voltage Doubling AC-DC Converter with Offset-Controlled Comparators for Piezoelectric Energy Harvester
	<i>Lianxi Liu, Wei Tu, Junchao Mu, Zhangming Zhu, Yintang Yang (School of Microelectronics, Xidian University)</i>
P1-44	0398: A Novel Stack Package Solution of AC-DC Chip for High-Power Density

	Adapters
	Jiaxing Wei, Jianfeng Wang, Ning Wang, Siyang Liu, Weifeng Sun (<i>National ASIC System Engineering Research Center, Southeast University</i>)
P1-45	0657: A Novel Start-up Circuit for boost DC-DC Converter with Synchronous Power-switch Current-limit
	Yanming Li, Hao Zhang, Hong Chai, Kaikai Wu, Changbao Wen(<i>School of Electronic and Control Engineering, Chang'an University</i>)
P1-46	0676: A Novel Adaptive CMOS Low-dropout Regulator with 3A Sink/Source Capability
	Yan Yang(<i>Institute of Microelectronics, Chinese Academy of Sciences, School of Telecommunication Engineering, Chengdu University of Information Technology</i>), Qi Wang, Yu Wang, Liyin Fu, Zongliang Huo(<i>Institute of Microelectronics, Chinese Academy of Sciences</i>)
P1-48	0331: Tunable Voltage-Mode Four Inputs Universal Biquad Using Three DVCCs
	Jiun-Wei Horng, Tung-Hsien Chan, Toung-Yi Li (<i>Department of Electronic Engineering, Chung Yuan Christian University</i>)
P1-49	0355: A 8.1 mW 0.1~2 GHz inductorless CMOS LNTA for software-defined radio applications
	Benqing Guo, Jun Chen, Yao Wang, Haiyan Jin, Guangjun Wen (<i>Centre for RFIC and System Technology, School of Communication and Information Engineering, University of Electronic Science and Technology of China</i>)
P1-50	0468: Analysis and Design of a High Linearity Quadrature Demodulator Based on SiGe BiCMOS Process
	Yadi Guo, Renyuan Chang, Jun Fu, Baoyong Chi, Yudong Wang(<i>Department of Microelectronics, Tsinghua University</i>)
P1-51	0569: A 2.4GHz Low Noise High Linearity RF Front-end Design
	Zhijian Chen, Min Cai, Ken Xu, Weiguo Zheng(<i>School of Electronic and Information Engineering, South China University of Technology</i>)
P1-52	0636: A 0.1-1.5G SDR Transmitter with Two-Stage Harmonic Rejection Power Mixer in 65-nm CMOS
	Bing Lyu, Yun Yin, Xiaobao Yu, Baoyong Chi(<i>Institute of Microelectronics, Tsinghua University</i>)
P1-53	0650: Self-recovering Short-circuit Protection Circuit for RF Class-D Power Amplifier
	Zheng Sun, Wei Ding, Yong Xu, Ying Huang(<i>Institute of Communication Engineering, PLA UST</i>), Guangyan Ma(<i>Institute of Field Engineering, PLA UST</i>), Yuanliang

	Wu(<i>Institute of Communication Engineering, PLA UST</i>)
P1-54	0730: An Automatic DC-Offset Cancellation Method and Circuit for RF Transceivers Ken Xu(<i>School of Electronic and Information Engineering, South China University of Technology, Rising Micro Electronics Co., Ltd.</i>), Min Cai, Xiaoyong He, Zhijian Chen, Weiguo Zheng(<i>School of Electronic and Information Engineering, South China University of Technology</i>)
P1-55	0756: A 2.4 GHz two-point Δ-Σ modulator with gain calibration and AFC for WPAN/BAN applications Chao Yang, Shaoquan Gao, Jingjing Dong, Hanjun Jiang, Woogeun Rhee, Zhihua Wang(<i>Institute of Microelectronics, Tsinghua University</i>)
P1-56	0765: A Wide Range PWM Signal Frequency Converter With the Identical Duty Cycle Jiangping He(<i>Department of Microelectronics, University of Electronic Science and Technology of China</i>), Jiang Sun(<i>Southwest Jiaotong University</i>), Bo Zhang(<i>Department of Microelectronics, University of Electronic Science and Technology of China</i>)
P1-57	0339: A 10b, 0.7ps Resolution Coarse-Fine Time-to-Digital Converter in 65nm CMOS using a Time residue Amplifier Jiyu Chen (<i>Shenzhen Graduate School, Peking University, Institute of Microelectronics, Peking University</i>), Song Jia, Yuan Wang(<i>Institute of Microelectronics, Peking University</i>)
P1-58	0372: A PVT-insensitive all digital CMOS time-to-digital converter based on looped delay-line with extension scheme Siliang Hua, Donghui Wang(<i>Key Laboratory of Information Technology for Autonomous Underwater Vehicles, Chinese Academy of Sciences</i>), Leiou Wang(<i>Key Laboratory of Information Technology for Autonomous Underwater Vehicles, Chinese Academy of Sciences, University of Chinese Academy of Sciences</i>), Yan Liu(<i>Key Laboratory of Information Technology for Autonomous Underwater Vehicles, Chinese Academy of Sciences</i>), Jiarui Li(<i>Key Laboratory of Information Technology for Autonomous Underwater Vehicles, Chinese Academy of Sciences, University of Chinese Academy of Sciences</i>)
P1-59	0405: A CMOS Charge Pump with Dual Compensation Amplifiers for Phase-Locked Loops Synthesizer Litong Nie, Zhigong Wang, Lu Tang, Junliang Wang (<i>Institute of RF- & OE-ICs, Southeast University</i>), Luosi Gao (<i>College of Electronics, Nanjing University of Posts and Telecommunications</i>)
P1-60	0484: Algorithms Based on All-Digital Phase-Locked Loop for Fast-locking and

	Spur Free
	Wei Xu , Wei Li(<i>State Key Laboratory of ASIC and Systems, Fudan University</i>)
P1-61	0518: A 1-V 5.2-5.7 GHz Low Noise Sub-Sampling Phase Locked Loop in 0.18 μm CMOS
	Jincheng Yang, Zhao Zhang, Peng Feng, Liyuan Liu, Nanjian Wu(<i>State Key Laboratory of Super Lattice and Microstructures, Chinese Academy of Sciences</i>)
P1-62	0543: A novel clock synchronizer for low-voltage clock distribution network
	Chong Lu(<i>SYSU-CMU Shunde International Joint Research Institute, Sun Yat-sen University, School of Information Science and Technology, Sun Yat-sen University</i>), Zhikui Duan(<i>School of Information Science and Technology, Sun Yat-sen University</i>), Yi Ding(<i>School of Computer Science and Technology, Hunan University of Arts and Science</i>), Hongzhou Tan(<i>SYSU-CMU Shunde International Joint Research Institute, Sun Yat-sen University, School of Information Science and Technology, Sun Yat-sen University</i>)
P1-63	0709: A Reference-Less All-Digital Burst-Mode CDR with Embedded TDC
	Mengyin Jiang, Yuan Wang, Baoguang Liu, Yuequan Liu, Song Jia, Xing Zhang(<i>Key Laboratory of Microelectronic Devices and Circuits (MoE), Institute of Microelectronics, Peking University</i>)
P1-64	0721: Four-bit Transient-to-Digital Converter with a Single RC-Based Detection Circuit for System-Level ESD Protection
	Nan Han, Yuan Wang, Guangyi Lu, Jian Cao, Xing Zhang(<i>Key Laboratory of Microelectronic Devices and Circuits (MoE), Institute of Microelectronics, Peking University</i>)
P1-65	0744: An Asynchronous Delay Line TDC for ADPLL in 0.13um CMOS
	Chunhui Li, Lei Ma, Junhui Xiang, Hao Min(<i>ASIC & System State Key Laboratory, AUTO-ID Laboratory of Fudan University</i>)
P1-66	0768: Analysis and design of quickly starting crystal oscillator
	Weiguo Zheng, Min Cai, Xiaoyong He, Ken Xu, Zhijian Chen(<i>School of Electronics and Information, South China University of Technology</i>)
P1-67	0771: Low Voltage Adaptive Delay Clock Buffer Design
	Yafei Liu, Xiangyu Li(<i>Institute of Microelectronics, Tsinghua University</i>)
P1-68	0333: A New Reading Scheme for Multitime Programmable (MTP) Memory Cells
	Cong Li, Jiancheng Li, Wenxiao Li, Shunqiang Xu, Yaling Chen(<i>School of Electronic Science and Engineering, National University of Defense Technology</i>)

P1-69	0345: Design and Implementation of Precise Measuring Method for the Access Time of Embedded Memory
	Yuqing Hu, Lijun Zhang, Youzhong Li, Qixiao Zhang, Erliang Li, Wei Jiang(<i>School of urban rail transportation, Soochow University</i>)
P1-70	0546: Impacts of External Magnetic Field and High Temperature Disturbance on MRAM Reliability Based on FPGA Test Platform
	Kai Yang, Yanqing Zhao, Jianguo Yang, Xiaoyong Xue, Yinyin Lin(<i>ASIC and System State Key Lab, Fudan University</i>), Jun-Soo Bae(<i>Semiconductor R & D Center, Samsung Electronics Co., Ltd</i>)
P1-71	0557: Design and testing of CMOS compatible EEPROM
	Haibin Yin, Xiaohong Peng(<i>VLSI and System Lab, Beijing University of Technology</i>), Peiyuan Wan(<i>Beijing Embedded System Key Lab, Beijing University of Technology</i>), Jinhui Wang(<i>VLSI and System Lab, Beijing University of Technology, Department of Electrical and Computer Engineering, North Dakota State University</i>), Ligang Hou(<i>VLSI and System Lab, Beijing University of Technology</i>)
P1-72	0621: Data pre-emphasis based retention reliability enhance scheme for MLC NAND Flash memories
	Haozhi Ma, Zhongyi Gao(<i>Institute of Microelectronics of the Tsinghua University</i>), Liyang Pan, Jun Xu(<i>Institute of Microelectronics of the Tsinghua University, Tsinghua National Laboratory for Information Science and Technology</i>)
P1-73	0655: Novel CMOS Technology Compatible Nonvolatile on-chip Hybrid Memory
	Zezhong Yang, Jinhui Wang(<i>VLSI and System Lab, Beijing University of Technology, Department of Electrical and Computer Engineering, North Dakota State University</i>), Ligang Hou(<i>VLSI and System Lab, Beijing University of Technology</i>), Na Gong(<i>Department of Electrical and Computer Engineering, North Dakota State University</i>)
P1-74	0522: Reusable IO Technique for Improved Utility of IC Test Circuit Area
	Junteng Zhang, Jinhui Wang, Ligang Hou(<i>VLSI and System Lab, Beijing University of Technology</i>), Na Gong(<i>Dept. of Electrical and Computer Engineering, North Dakota State University</i>)

Thursday

Thursday, November 5, 8: 30 – 10: 00

Thursday, November 5, 8: 30 – 10: 00

Wufu Hall

Keynote Session K-5 & K-6

Wufu Building1F

K-5 The Hype, Myths, and Realities of 3D Integration and Design-for-Test (8: 30-9: 15)

Prof. Krishnendu Chakrabarty (Duke University, USA)

K-6 Whole-Chip ESD Design Verification by CAD: Challenges & Solutions(9: 15-10: 00)

Prof. Albert Wang(University of California, Riverside, USA)

Thursday, November 5, 10: 15 – 12: 15

Thursday, November 5, 10: 15 – 12: 15	Maesai Reception Hall Wangjiang Club 1F
Session A3 : Implantable Device & IoT	
Session Chair : Yumei Huang, <i>Fudan University</i>	

	Title
A3-1	0642: Motion Artifact Removal Based on ICA for Ambulatory ECG Monitoring
10: 15	Shudong Tian, Jun Han, Jianwei Yang, Lijun Zhou, Xiaoyang Zeng (<i>State Key Laboratory of ASIC & System, Fudan University</i>)
A3-2	0772: A High Input Impedance AC-Coupled SoC Suitable For Wearable ExG Monitor
10: 30	Yubin Zhang, Yajie Qin, Han Jin (<i>State Key Laboratory of ASIC & System, Fudan University, Shanghai</i>)
A3-3	0595: An Inductive Wireless Telemetry Circuit with OOK Modulation for Implantable Cardiac Pacemakers
10: 45	Chong Guo, Hong Zhang, Zhouyi Ma, Jie Zhang, Jie Lin, Ruizhi Zhang (<i>Department of Microelectronics, Xi'an Jiaotong University</i>)
A3-4	0444: A Low Power Potentiostat for Implantable Glucose Sensor Tag
11: 00	Xi Tan, Sizheng Chen, Zhibin Xiao, Junyu Wang (<i>ASIC & System State Key Laboratory, Fudan University</i>), Feng Chen (<i>Information Center of China State Food and Drug Administration (CFDA)</i>)
A3-5	0699: Small-Sized and Noise-Reducing Power Analyzer Design for Low-Power IoT Devices
11: 15	Ryosuke Kitayamay, Masao Yanagisaway, Nozomu Togaway (<i>Department of Computer Science and Engineering, Waseda University</i>) Takashi Takenakaz(<i>Green Platform Laboratories, NEC Corporation</i>)
A3-6	0755: Driver Circuit System for Temperature Control of Micro-hotplates: Measurement and Strategy
11: 30	Jiarui Wu, Jun Yu, Jiaming Liang, Zhan Shi, Zhongzhou Li, Zhenan Tang(<i>School of Electronic Science & Technology, Dalian University of Technology, Liaoning IC Technology Key Lab</i>)

Thursday, November 5, 10: 15 – 12: 15	Brunei Meeting Room Wangjiang Club 2F
Session B3 : Signal Processing & Filter	
Session Chair : Hongbin Sun, <i>Xi'an Jiaotong University</i>	

	Title
B3-1	0348: A High-speed and Area-efficient Sign Detector for Three Moduli Set RNS

	{2^n, 2^{n-1}, 2^{n+1}} (Invited paper)
10: 15	Sachin Kumar, Chip-Hong Chang (<i>School of Electrical and Electronic Engineering, Nanyang Technological University</i>)
B3-2	0414: Ultra-Short Length Stochastic Computation Based on Multiple Partition Computing
10: 45	Jienan Chen, Jianhao Hu, Jiangyun Zhou (<i>University of Electronic Science and Technology of China</i>)
B3-3	0660: New Design for Low Complexity and Low Power Partial Programmable Shifters
11: 00	Yujia Wang (<i>Undergraduate student, Singapore University of Technology and Design</i>), Jiajia Chen (<i>Pillar of Engineering Product Development, Singapore University of Technology and Design</i>)
B3-4	0402: Full-Digital High Throughput Design of Adaptive Decision Feedback Equalizers Using Coefficient-Lookahead
11: 15	Wen-Quan He, Yu-Chun Lin, Jui-Yi Hung, Shyh-Jye Jou (<i>Department of Electronics Engineering, National Chiao Tung University</i>)
B3-5	0346: Flat Passband Gain Design Algorithm for 2nd-order RC Polyphase Filter
11: 30	Yoshiki Niki, Shu Sasaki, Nobu Yamaguchi, Jian Kang, Takashi Kitahara, Haruo Kobayashi (<i>Division of Electronics and Informatics, Gunma University</i>)
B3-6	0393: Automatic Design of Doubly-terminated RC Polyphase Filters by Using Distributed Genetic Algorithm
11: 45	Yoshiki Sugawara, Nobukazu Takai, Masato Kato, Hiroaki Seki, Kento Suzuki, Haruo Kobayashi (<i>Department of Electronic Eng., Gunma University</i>)

Thursday, November 5, 10: 15 – 12: 15	Penang Island Meeting Room
Session C3 : Flash & Pipelined ADC	Wangjiang Club 2F
Session Chair : Qi Yu, University of Electronic Science and Technology of China	

	Title
C3-1	0788: A Novel Power Optimization Mechanism for Pipelined ADCs (invited paper)
10: 15	Xiaojin Fu, He Tang (<i>School of Microelectronics and Solid-State Electronics, University of Electronic Science and Technology of China</i>)
C3-2	0566: A 100-MS/s 5-bit Fully Digital Flash ADC With Standard Cells
10: 45	Xiangyan Xue, Xuerong Zhou, Fan Ye, Junyan Ren (<i>State Key Laboratory of ASIC and System, Fudan University</i>)
C3-3	0630: A 1.5-GS/s 5-bit Interpolating ADC with Offset Averaging and

	Interpolating Sharing Resistors Network
11: 00	Rongjin Xu, Yongzhen Chen, Mingshuo Wang (<i>State Key Laboratory of ASIC and Systems, Fudan University</i>), Ning Li, Fan Ye, Junyan Ren (<i>State Key Laboratory of ASIC and Systems, Fudan University, Department of Microelectronics, Fudan University</i>)
C3-4	0689: A High-Speed analog front-end circuit used in a 12bit 1GSps Pipeline ADC
11: 15	Meng Ni, Fule Li, Weitao Li, Chun Zhang, Zhihua Wang (<i>Tsinghua National Laboratory for Information Science and Technology Institute of Microelectronic, Tsinghua University</i>)
C3-5	0714: Sample-hold Circuit and Stage Circuits in a Traditional 12-b 80-Msample/s Pipelined A/D Converter
11: 30	Xiang Jiang, Jun Cheng, Ting Zhang, Liao Gong, Qiyun Ma (<i>Department of Microelectronics, Xi'anJiaotong University</i>), Liang Li (<i>Science and Technology on Analog Integrated Circuit Laboratory</i>)
C3-6	0471: A 2-V 40-MS/s 14-bit Pipelined ADC for CMOS image sensor
11: 45	Teng Chen, Leli Peng, Haibin Li, Ning Ding, Yuchun Chang (<i>State Key Laboratory on Integrated Optoelectronics, College of Electronic Science and Engineering, Jilin University</i>), Cheng Ma (<i>State Key Laboratory on Integrated Optoelectronics, College of Electronic Science and Engineering, Jilin University, Gpixel Inc, Changchun</i>)
C3-7	0324: Split-Based 200Msps and 12 bit ADC Design
12: 00	Haijun Lin (<i>School of Optoelectronics and Communication Engineering, Xiamen University of Technology</i>), Xiao Yang (<i>College of Information Science and Engineering, Huaqiao University, Xiamen, China</i>)

Thursday, November 5,10: 15 – 12: 15	Penang Meeting Room
Session D3 : Reliability & Other Device Topics	Wangjiang Club 2F
Session Chair : Carol (Rouying) Zhan, Freescale Semiconductor	

	Title
D3-1	0362: NBTI prediction and its induced time dependent variation (invited paper)
10: 15	Jian F. Zhang, Meng Duan, Zhigang Ji, Weidong Zhang (<i>School of Engineering, Liverpool John Moores University</i>)
D3-2	0426: Overshoot Stress Impact on HfO₂ High-k Layer Dynamic SILC (invited paper)
10: 45	Guangxing Wan, Shuxiang Zhang, (<i>South University of Science and Technology of China, Institute of Microelectronics, Chinese Academy of Sciences</i>) Lingli Jiang, Tianli Duan, Hongyu Yu, (<i>South University of Science and Technology of China, Institute of Microelectronics</i>) Bo Tang, Chao Zhao, Huilong Zhu (<i>Chinese Academy of Sciences</i>)

D3-3	0472: A Study on HCI Induced Gate Leakage Current Model Used for Reliability Simulations in 90nm n-MOSFETs
11: 15	Nobukazu Tsukiji, Hitoshi Aoki, Masaki Kazumi, Takuya Totsuka, Masashi Higashino, Haruo Kobayashi (<i>Department of Electronics and Informatics, Graduate School of Science and Technology, Gunma University</i>)
D3-4	0385: Study on Maximum Electric Field Modeling Used for HCI Induced Degradation Characteristic of LDMOS Transistors
11: 27	Masashi Higashino, Hitoshi Aoki, Nobukazu Tsukiji, Masaki Kazumi, Takuya Totsuka, Haruo Kobayashi (<i>Department of Electronic Eng., Gunma Gunma University</i>)
D3-5	0467: Dependency of Current Collapse on the Device Structure of GaN-based HEMTs
11: 39	Xingye Zhou, Zhihong Feng, Yuanjie Lv, Xin Tan, Yuangang Wang, Guodong Gu, Xubo Song, Peng Xu, Shaobo Dun, Shujun Cai (<i>National Key Laboratory of ASIC, Hebei Semiconductor Research Institut</i>)
D3-6	0536: A physical model of novel UV and blue-extended photodetector based on CMOS process
11: 51	Xiangliang Jin, Manfang Tian, Zhenyu Jiang, Han Wang (<i>School of Physics and Optoelectronics, Xiangtan University, Hunan Engineering Laboratory for Microelectronics, Optoelectronics and System on A Chip</i>)
D3-7	0577: Simulation and Analysis of P+/N SPAD for 3D Imaging
12: 03	Hongjiao Yang, Xiangliang Jin, Lizhen Tang, Weihui Liu, Jia Yang (<i>Faculty of Physics and Optoelectronic Engineering, Xiangtan University, Hunan Engineering Laboratory for Microelectronics, Optoelectronics and System on a Chip</i>)

Thursday, November 5, 13: 30 – 15: 30

Thursday, November 5, 13: 30 – 15: 30

Maesai Reception Hall

Session A4 : Micro Processor & NOC

Wangjiang Club 1F

Session Chair : Xiaofang Zhou, Fudan University

	Title
A4-1	0363: A Novel Routing Structure of Coarse-Grained Reconfigurable Architecture for Radar Application
13: 30	Bo Liu, Yu Gong (<i>National ASIC System Engineering Technology Research Center Southeast University</i>) Dongming Zhang, Weiqi Ge (<i>Integrated Circuits Technology Research Institute Southeast University</i>)

A4-2	0646: Exploring Stacked Main Memory Architecture for 3D GPGPUs
13: 45	Yuang Zhang (<i>Institute of VLSI Design, LAPEM, Nanjing University, Department of Electronic Systems, KTH-Royal Institute of Technology</i>), Li Li, Minglun Gao, Yuxiang Fu, Hongbing Pan (<i>Institute of VLSI Design, LAPEM, Nanjing University</i>), Axel Jantsch (<i>Institute of Computer Technology, Vienna University of Technology</i>), Zhonghai Lu (<i>Department of Electronic Systems, KTH-Royal Institute of Technology</i>)
A4-3	0491: Lagrangian Relaxation Based Topology Synthesis for Application-Specific Network-on-Chips
14: 00	Jinglei Huang, Zhigang Li, Wei Zhong, Song Chen (<i>Department of Electronic Sci. & Tech., University of Science and Technology of China</i>)
A4-4	0494: A Network Components Insertion Method for 3D Application-Specific Network-on-Chip
14: 15	RongRong Zhou, Fen Ge, Gui Feng, Ning Wu (<i>College of Electronic and Information Engineering Nanjing University of Aeronautics and Astronautics</i>)
A4-5	0679: An Inclusive Fault Model for Network-on-Chip
14: 30	Yi He, Gensheng Chen (<i>State Key Lab of ASIC and System, Fudan University</i>)
A4-6	0303: An Efficient Low Power & High Performance in MPSOC
14: 45	B. Naresh Kumar Reddy, Dheeraj Sharma, Y.B. Nithin Kumar, M.H. Vasanth (Dept. of Electronics and Communication Engineering)
A4-7	0383: A Novel Configuration Context Cache Structure of Reconfigurable Systems
15: 00	Yu Gong, Bo Liu, Chen Mei (<i>National ASIC System Engineering Technology Research Center, Southeast University, Nanjing</i>), Ruihe Wang (<i>Integrated Circuits Technology Research Institute, Southeast University, Wuxi</i>)
A4-8	0767: Design of a Dynamically Reconfigurable Arithmetic Units for Matrix Algorithms
15: 15	Weijiang Wang, Yingtao Ding, Shan Cao, Xianli Zhao (<i>School of Information and Electronics, Beijing Institute of Technology</i>)

Thursday, November 5, 13: 30 – 15: 30	Brunei Meeting Room
Session B4 : Circuit Optimization and Physical Design Automation	
	Wangjiang Club 2F

Session Chair : Hai Wang, *University of Electronic Science and Technology of China*

	Title
B4-1	0742: Design and Optimization of Asynchronous Circuits with Gate-level Pipelining (invited paper)
13: 30	Makoto Ikeda (<i>Department of Electric Engineering and Information Systems, the University of Tokyo</i>)

B4-2	0376: An Adaptive Dynamical Low-Rank Tensor Approximation Scheme for Fast Circuit Simulation (invited paper)
14: 00	Kim Batselier, Quan Chen, Ngai Wong (<i>Department of Electrical and Electronic Engineering The University of Hong Kong</i>)
B4-3	0394: Comparator Circuits Automation by Combination of Distributed Genetic Algorithm and HSPICE Optimization
14: 30	Kento Suzuki, Nobukazu Takai, Masato Kato, Hiroaki Seki, Yoshiki Sugawara, Haruo Kobayashi (<i>Department of Electronics Eng., Gunma University</i>)
B4-4	0460: LC-KO: A Congestion-Aware and Area & Timing-Oriented Placement Method
14: 42	Zhixiong Di, Qianyin Xiang, Quanyuan Feng (<i>The School of Information Science and Technology, Southwest Jiaotong University</i>) Yanlong Wang (<i>MARVELL</i>), Shuang Qiao (<i>NVIDIA</i>)
B4-5	0529: A VLSI Global Placement Solver Based on Proximal Alternating Direction Method
14: 54	Jianli Chen, Zheng Peng, Wenxing Zhu (<i>Center for Discrete Mathematics and Theoretical Computer Science, Fuzhou University</i>)
B4-6	0562: DPALS: A Dynamic Programming-based Algorithm for Two-level Approximate Logic Synthesis
15: 06	Chen Zou (<i>The State Key Lab of ASIC & System, Fudan University</i>), Weikang Qian (<i>UM-SJTU Joint Institute, Shanghai Jiao Tong University</i>), Jie Han (<i>Department of Electrical and Computer Engineering, University of Alberta</i>)
B4-7	0625: Improved Monitoring-Path Selection Algorithm for Suspicious Timing Error Prediction based Timing Speculation
15: 18	Shinnosuke Yoshida, Youhua Shi, Masao Yanagisawa, Nozomu Togawa (<i>Department of Computer Science and Communications Engineering, Waseda University</i>)

Thursday, November 5, 13: 30 – 15: 30	Penang Island Meeting Room
Session C4 : RF Circuit 2	Wangjiang Club 2F
Session Chair : Yann Deval, <i>University of Bordeaux, Talence, France</i>	

	Title
C4-1	0311: A 28-Gb/s 60-GHz Wireless Transceiver in 65nm CMOS with 64QAM Capability (invited paper)
13: 30	Kenichi Okada (<i>Tokyo Institute of Technology, Ookayama, Meguro-ku, Tokyo , Japan</i>)
C4-2	0516: An All-Digital Quadrature RF Transmitter with 8-bit $\Sigma \Delta$ Modulation

14: 00	Pan Xue, Yilei Shen, Yang Zhao, Zhiliang Hong (<i>State Key Laboratory of ASIC & System, Fudan University, Shanghai, China</i>)
C4-3	0420: A 30-GHz to 39-GHz mm-Wave Low-power Injection-locked Frequency Divider in 65nm CMOS
14: 13	Guangyao Zhou, Shunli Ma, Fazhi An (<i>State Key Laboratory of ASIC and System, Fudan University, Shanghai, China</i>)Ning Li, Fan Ye, Junyan Ren (<i>State Key Laboratory of ASIC and System, Fudan University, Shanghai, China, Department of Microelectronics, Fudan University, Shanghai, China</i>)
C4-4	0575: A 39GHz - 80GHz millimeter-wave frequency doubler with low power consumption in 65nm CMOS technology
14: 26	Qian Chen, Fazhi An, Guangyao Zhou, Shunli Ma, Fan Ye, Junyan Ren (<i>State Key Laboratory of ASIC and System, Fudan University, Shanghai, China</i>)
C4-5	0610: A Wide-division-ratio 100MHz-to-5GHz Multi-Modulus Divider Chain for Wide-band PLL
14: 39	Fazhi An, Shunli Ma, Qian Chen, Guangyao Zhou, Fan Ye, Junyan Ren (<i>State Key Laboratory of ASIC and System, Fudan University, Shanghai , China</i>)
C4-6	0738: A Programmable Divider with Wide Division Range Applied in An FMCW Frequency Synthesizer
14: 52	Dan Wu,Wei Li (<i>State Key Laboratory of ASIC & System, Fudan University</i>)
C4-7	0661: A Reconfigurable Analog Baseband for Low-Power Wi-Fi Receiver
15: 05	Jiachen Hao, Zheng Song, Baoyong Chi (<i>Institute of Microelectronics, Tsinghua University, Beijing, China</i>)
C4-8	0359: A 0.06 mm² 6 dBm IB_{1dB} wideband CMOS class-AB LNTA for SAW-less applications
15: 18	Jun Chen, Benqing Guo, Boyang Zhang, Guangjun Wen (<i>School of Communication and Information Engineering, University of Electronic Science and Technology of China, Chengdu, China</i>)

Thursday, November 5, 13: 30 – 15: 30	Penang Meeting Room
Session D4 : Memory 1	Wangjiang Club 2F
Session Chair : Sarfraz Khawar,	
<i>The Hong Kong University of Science and Technology</i>	

	Title
D4-1	0369: Nanosecond-Order Fast Switching and Ultra-Multilevel Storage in Lateral GeTe and Ge₁Sb₄Te₇-Based Phase-Change Memories (invited paper)
13: 30	YouYin, and Sumio Hosaka (<i>Division of Electronics and Informatics, Gunma University, Kiryu, Gunma, Japan</i>)

D4-2	0400: Spin Orbit Torques for ultra-low Power Computing (invited paper)
14: 00	Kaihua Cao, Heng Zhao, Mengxing Wang (<i>Fert Beijing Institute, Beihang University, 100191, Beijing, P.R. China</i>) Weisheng Zhao (<i>Fert Beijing Institute, Beihang University, 100191, Beijing, P.R. China, IEF, Univ. Paris Sud, 91405 Orsay, France, UMR 8622, CNRS, 91405 Orsay, France</i>)
D4-3	0589: Influence of Nitrogen Buffering on Oxygen in ITO-Capped Resistive Random Access Memory with NH3 Treatment
14: 30	Ji Chen, Jen-Chung Lou(<i>School of Software and Microelectronics, Peking University, Beijing , China</i>) Kuan-Chang Chang, , Tsung-Ming Tsai, Chih-Hung Pan (<i>Department of Materials and Optoelectronic Science, National Sun Yat -Sen University, Kaohsiung 804, Taiwan</i>) Ting-Chang Chang (<i>Department of Physics, National Sun Yat-Sen University, Kaohsiung 804, Taiwan</i>)
D4-4	0410: Study of Limiting Upset Cross-section of DICE Latch in Aerospace SoC
14: 45	Zhu Ming, Zhang Lei, Zhang Wei (<i>China Academy of Space Technology, Beijing, China</i>)

Thursday, November 5, 15: 45 – 17: 45

Thursday, November 5, 15: 45 – 17: 45	Maesai Reception Hall
Special Session : THz Communication and Sensing	Wangjiang Club 1F
Session Chair : Xiwei Huang, Hangzhou Dianzi University	

	Title
A5-1	0787: Survey and Statistical Analysis of THz Detectors (Invited paper)
15: 45	Xu-Guang Li, Dong Yan, Hai-Peng Fu, Jian-Guo Ma (<i>School of Electronic Information Engineering, Tianjin University,</i>)
A5-2	0791: A 60-GHz Wireless Transceiver with Dual-Mode Power Amplifier for IEEE 802.11ad in 65nm CMOS (Invited paper)
16: 10	Baoyong Chi, Lixue Kuang, Haikun Jia, Zhiping Wang, Zhihua Wang (<i>Institute of Microelectronics, Tsinghua University, Beijing, Tsinghua National Laboratory for Information Science and Technology</i>)
A5-3	Speak Only: Passive Circuits for MM-Wave and THz Application (Invited paper)
16: 35	Xun Luo (<i>University of Electronic Science and Technology of China</i>)
A5-4	0780: A CMOS THz Transceiver based Spectroscopy towards Label-free DNA Sequencing (Invited paper)
17: 00	Xiwei Huang, Liangling Sun (<i>Ministry of Education Key Lab of RF Circuits and Systems, Hangzhou Dianzi University</i>) Yu Jiang, Hao Yu (<i>School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore</i>) Yang Shang (<i>Advantest Pte</i>)

	<i>Ltd, Singapore)</i>
A5-5	0799: D-Band Down Conversion Chipset with I-Q Outputs Using 0.13-μm SiGe BiCMOS Technology (Invited paper)
17: 25	Xiao-Dong Deng (<i>Ministry Key Laboratory of JGMT, Nanjing University of Science and Technology (NUST), Nanjing, Semiconductor Device Research Laboratory, Terahertz Research Centre, CAEP, Chengdu</i>) Yihu Li, Yong-Zhong Xiong (<i>Semiconductor Device Research Laboratory, Terahertz Research Centre, CAEP, Chengdu</i>) Wen Wu (<i>Ministry Key Laboratory of JGMT, Nanjing University of Science and Technology (NUST), Nanjing</i>)

Thursday, November 5, 15: 45 – 17: 45	Brunei Meeting Room
Session B5 : Chip Test & Reliability	Wangjiang Club 2F
Session Chair : Min Ren, University of Electronic Science and Technology of China	

	Title
B5-1	0775: Distinguishing Dynamic Bridging Faults and Transition Delay Faults (invited paper)
15: 45	Cheng-Hung Wu, Saint James Lee and Kuen-Jong Lee (<i>Dept. of EE, National Cheng Kung University, Taiwan</i>)
B5-2	0789: An Enhanced Built-In Self-Repair Technique for Yield and Reliability Improvement of Embedded Memories (invited paper)
16: 12	Shyue-Kung Lu, Hao-Wei Lin (<i>Dept. Electrical Engineering, National Taiwan University of Science and Technology, Taipei, Taiwan</i>), Masaki Hashizume (<i>Institute of Technology and Science, The University of Tokushima, Tokushima, Japan</i>)
B5-3	0396: Power Supply Noise and Its Reduction in At-Speed Scan Testing (invited paper)
16: 39	Xiaoqing Wen (<i>Department of Computer Systems and Engineering, Kyushu Institute of Technology, Kawazu , Izuka, Japan</i>)
B5-4	0305: Electrical Overstress (EOS): Challenges for Component and System-Level Co-Design (invited paper)
17: 06	Steven H. Voldman (<i>IEEE Fellow, Dr Steven H. Voldman LLC</i>)
B5-5	0753: A Low-Leakage Power Clamp ESD Protection Circuit with Prolonged ESD Discharge Time and Compact Detection Network
17: 33	Jian Cao , Xing Zhang (<i>School of Software and Microelectronics, Peking University, Beijing, China, Institute of Microelectronics, Peking University, Beijing, China</i>) Zhenxu Ye (<i>School of Software and Microelectronics, Peking University, Beijing, China</i>) Yuan Wang, Guangyi Lu (<i>Institute of Microelectronics, Peking University, Beijing, China</i>)

Thursday, November 5, 15: 45 – 17: 45

Penang Island Meeting Room

Session C5 : Analog Circuit

Wangjiang Club 2F

Session Chair : Ziqiang Wang, Tsinghua University

	Title
C5-1	0521: Future Low-Noise Technologies for RF, Analog and Mixed-Signal Integrated Circuits (invited paper)
15: 45	Chih-Hung Chen, Xuesong Chen (<i>Department of Electrical and Computer Engineering, McMaster University, Hamilton, ON, CANADA</i>) D. Y. Wu, and Chao Sheng Chen (<i>United Microelectronics Corporation (UMC), Hsinchu, Taiwan, R.O.C.</i>)
C5-2	0774: A High-Slew Rate Rail-to-Rail Operational Amplifier by Flipped Voltage Followers (invited paper)
16: 09	Shu-Hang Zhang, Yu-Cheng Feng, Miin-Shyue Shiau, Don-Gey Liu (<i>Department of Electronic Engineering, Feng Chia University, Taichung, Taiwan, R.O.C</i>) Qi-Ming Wan (<i>School of Information Engineering, Zhongshan Polytechnic, Zhongshan, Guangdong</i>)
C5-3	0782: Low-Voltage CMOS DC-DC Converters for Energy Harvesting Applications (invited paper)
16: 33	Zehua Chen, Weiyin Wang (<i>Department of Information Science and Electronic Engineering, Zhejiang University, Hangzhou, China</i>), Hei Wong (<i>Department of Information Science and Electronic Engineering, Zhejiang University, Hangzhou, China; Department of Electronic Engineering, City University of Hong Kong, Kowloon, Hong Kong, China</i>)
C5-4	0479: Hybrid LED Driver for Multi-Channel Output with High Consistency
16: 57	D.J.Yu, Q. Yu, Ning Ning and Y. Liu (<i>State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu, P. R. China</i>) Z.Y.Shi (<i>Science and Technology on Reliability Physics and Application Technology of Electronic Component Laboratory, Guangzhou 510610, Guangdong, P. R. China</i>)
C5-6	0461: A Low-Power Continuous-time Comparator with Enhanced Bias Current at the Flip Point
17: 21	Hongyi Wang, Yanjiao Du, Xu Jia, Youyou Fan (<i>Department of Microelectronics, Xi'an Jiaotong University</i>)
C5-7	0462: Design of Novel Chopper Stabilized Rail-to-Rail Operational Amplifier
17: 33	Yong Xu, Zheng Sun, Yuanliang Wu (<i>Institute of Communication Engineering, PLA University of Science and Technology</i>), Fei Zhao (<i>Institute of Command Information System, PLA University of Science and Technology</i>)

Thursday, November 5, 15: 45 – 17: 45

Penang Meeting Room

Session D5 : High Power Device

Wangjiang Club 2F

Session Chair : Ching-Ting Lee, *National Cheng Kung University*

	Title
D5-1	0332: 10 Mbps High-voltage Digital Transciever on Single Die for 50 V Voltage Swing (invited paper)
15: 45	Chua-Chin Wang, Senior Member, IEEE, and Min-Yu Tseng (<i>Department of Electrical Engineering, National Sun Yat-Sen University, Kaohsiung, Taiwan</i>)
D5-2	0797: Photoelectrochemically Recessed AlGaN/GaN Monolithic Inverter Incorporating LiNbO₃ Ferroelectric Film (invited paper)
16: 15	Ching-Ting Lee, Jhe-Hao Chang, Chun-Yen Tseng (<i>Institute of Microelectronics, Department of Electrical Engineering, National Cheng Kung University</i>)
D5-3	0560: Design of a High Voltage Gate Driver Module
16: 45	Longcheng Que, Jian Lv (<i>University of Electronic Science and Technology of China, Chengdu, China</i> , <i>University of Arkansas, Fayetteville, Arkansas, USA</i>) Simon S.Ang (<i>University of Arkansas, Fayetteville, Arkansas, USA</i>)
D5-4	0693: Low on-resistance Power MOSFET Design for Automotive Applications
17: 00	Tianhong Ye and Kuan W. A. Chee (<i>Department of Electrical and Electronic Engineering, University of Nottingham, Ningbo, Zhejiang, People's Republic of China</i>)
D5-5	0594: Novel Superjunction Collector Design of Power SiGe HBTs for High f_T×BVCEO×β Product
17: 15	Xiao Wang, Dongyue Jin, Wanrong Zhang, Xinyi Zhao, Yanling Guo, Qiang Fu (<i>College of Electronic Information and Control Engineering, Beijing University of Technology, Beijing, China</i>)
D5-6	0751: Modeling and Design of the LDMOSFET for RF power amplifier applications
17: 30	Ting Liu and Kuan W. A. CHEE (<i>Department of Electrical and Electronic Engineering, The University of Nottingham Ningbo China, Ningbo, Zhejiang, People's Republic of China</i>)

Thursday, November 5, 17: 45 – 18: 45

Thursday, November 5, 17: 45 – 18: 45

Wufu Hall

Post Session (II)

Wufu Building 1F

	Title
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P2-01	0440: A TSV Repair Method for Clustered Faults
	Shijie Zhang, Xiaole Cui, Qiang Zhang, Yufeng Jin(<i>Key Lab of Integrated Microsystems, Peking University Shenzhen Graduate School</i>)
P2-02	0448: Post-Bond Test for TSVs using Voltage Division
	Bingqiang Jing, Xiaole Cui, Yalin Ran , Yufeng Jin(<i>Key lab of Integrated Microsystems, Peking University Shenzhen Graduate School</i>)
P2-03	0449: An Effective Analytical 3D Placer in Monolithic 3D IC Designs
	Yande Jiang, Chang Liu, Yang Guo(<i>Institute of Microelectronics, National University of Defense Technology</i>) Xu He(<i>Institute of Microelectronics, National University of Defense Technology, Department of Computer Science and Engineering, The Chinese University of Hong Kong</i>)
P2-04	0623: The data Retention Improvement with 2T Structure OTP on 0.18um CMOS Technology
	Guanyu Chen, Feng Lin, Yongliang Gao, Chunxu Li, Duowu Wen, Zhe Zhang(<i>CSMC Technologies Corporation Wuxi</i>)
P2-05	0641: Fault Detection and Redundancy Design for TSVs in 3D ICs
	Sai Hu, Qin Wang, Zheng Guo, Jing Xie, Zhigang Mao(<i>Dept of Micro/nano-electronics, Shanghai Jiao Tong University</i>)
P2-06	0647: A Crosstalk Avoidance Scheme Based on Re-layout of Signal TSV
	Jiayi Hu, Qin Wang, Jianfei Jiang, Jing Xie, Zhigang Mao(<i>Department of Microelectronics and Nanoscience, Shanghai Jiao Tong University</i>)
P2-07	0312: A New Intrinsic Parameter Extraction Approach for Small-Signal Model of AlGaN/ GaN Devices
	Linghan Zhang, Yunzhou Wang, Yicong Liu, Xusheng Tang (<i>School of Information Science and Engineering, Southeast University</i>)
P2-08	0316: Performance Optimization of Conventional Schottky Barrier CNTFETs Based on Stair-Case Halo Doping Strategy
	Amin ghasemi nejad raeini, M.H. Shekari, H. Sadeghi(<i>Gol e Gohar Mining and industrial company</i>) Zoheir Kordrostami(<i>Department of Electrical and Electronic Engineering, Shiraz University of Technology</i>)
P2-09	0388: The Compact V_{th} Model for Biaxial Strained Si NMOSFET
	Yin Shujuan(<i>The college of science, Beijing Information Science and Technology University</i>)
P2-10	0488: Design of Explicit-pulse Generators with CNTFET
	Wang Qian, Wang Pengjun, Gong Daohui(<i>Institute of Circuits and Systems, Ningbo</i>)

	<i>University)</i>
P2-11	0504: Fabrication of 3.1kV/10A 4H-SiC Junction Barrier Schottky Diodes
	Chengsen Wang, Yidong Shen (<i>JieJie Microelectronics</i>) Hao Yuan, Xiaoyan Tang, Renxu Jia, Yuming Zhang, Yimen Zhang(<i>School of Microelectronics, Key Laboratory of Wide Band-Gap Semiconductor Materials and Devices,Xidian University</i>) Qingwen Song(<i>School of advanced materials and nanotechnology, Xidian University</i>)
P2-12	0525: Analytical Models for Threshold Voltage, Drain Induced Barrier Lowering Effect of Junctionless Triple-Gate FinFETs
	Guangxi Hu, Shuyan Hu, Jianhua Feng, Ran Liu, Lingli Wang, Lirong Zheng(<i>State Key laboratory of ASIC and system, School of Information Science and Technology,Fudan University</i>)
P2-13	0554: A novel SCR-LDMOS for high voltage ESD protection
	Deng Jing , Chen Xingbi (<i>State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China</i>)
P2-14	0658: Design consideration of uni-traveling carrier photodiode: influence of doping profile and buffer layer
	Yang Li, Hang Zhou(<i>The School of Electronic and Computer Engineering, Peking University Shenzhen Graduate School,Peking University</i>) Pengfei Xu, Yujie Chen, Yanfeng Zhang, Siyuan Yu(<i>State Key Laboratory of Optoelectronic Materials and Technologies, School of Microelectronics,Sun Yat-sen University</i>)
P2-15	0667: Deep Trench Junction Termination Employing Variable-K Dielectric for High voltage Devices
	Huan Li, Xingbi Chen(<i>State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology</i>)
P2-16	0668: Investigation of Line Tunnel Field Effect Transistor with Ge/Si Heterojunction
	Shuqin Zhang, Chunsheng Jiang, Libin Liu, Jing Wang, Jun Xu(<i>Tsinghua National Laboratory for Information Science and Technology, Institute of Microelectronics Tsinghua University</i>)
P2-17	0708: Investigation of Self-heating Effect in SOI tunnel Field-effect Transistor
	C. Qian, Mao-Lin Shi, Lin Chen, Q.Q. Sun, Peng Zhou, S. J. Ding , D. W. Zhang(<i>State Key Laboratory of ASIC and System, Schoolt of Microelectronics, Fudan University</i>)
P2-18	0722: Performance evaluation and Influence of Device Parameters on Threshold Voltage of Dual-material Strained Gate-all-around MOSFET
	Yefei Zhang, Zunchao Li, Qingzhi Meng, Yunhe Guan, Dongxu Luo(<i>Department of Microelectronics, Xi'an Jiaotong University</i>)

P2-19	0785: Using GIDL mechanism for Low-Power Consumption and Data Retention Time Improvement in a Double-Gate Nanowire TFT 1T-DRAM with Fin-Gate and Pillar-Body Structure
	Wei-Han Lee, Jyi-Tsong Lin, Yu-Chun Wang, Po-Hsieh Lin, Chien-Chia Lai, Yong-Huang Lin , Tin-Chun Chang(<i>Dept. of Electrical Engineering, National Sun Yat-Sen University</i>)
P2-20	0318: An Iterative Synthesis Method For Timing-driven Design
	Zhang Jie , Jin Lin(<i>IC Design Center, CETC No.38 Research Institute</i>)
P2-21	0338: A Peak Power Optimization Scheduling Algorithm for Single Cycle Operations and Multi-cycle Operations
	Sun Qiang (<i>Engineering college Mudanjiang Normal University</i>)
P2-22	0490: A Timing Failure Tolerance Design with In-Field Simultaneous Error Detection and Correction
	Ziyi Hao(<i>Institute of VLSI Design, Zhejiang University</i>) Xiaoyan Xiang, Chen Chen, Jianyi Meng(<i>Department of Microelectronics, Fudan University</i>)
P2-23	0547: A Simple Semi-analytical Parameter Extraction Method for 40nm Gate length MOSFET
	Panpan Yu, Ying Zhou, Jianjun Gao(<i>School of Information Science and Technology, East China Normal University</i>) Ling Sun(<i>Jiangsu Key Laboratory of ASIC Design, Nantong University</i>)
P2-24	0601: SPICE Model for Dual-Extended Memristor
	Zhiyuan Li, Qingkun Li(<i>School of Electronic Engineering, Heilongjiang University, Post-doctoral Mobile Stations of Electronic Science and technology, Heilongjiang University</i>) Dianzhong Wen(<i>School of Electronic Engineering, Heilongjiang University</i>)
P2-25	0640: PS-BloTAM: Pre-Sampling based Architecture-level Temperature Analysis Methodology
	Zou Tian, Luo Zuying(<i>Department of Information and Science Technology, Beijing Normal University</i>)
P2-26	0745: An Automatic Translation and Parallelization System for General Purpose Reconfigurable Processor
	Fenghuo Tian, Weiguang Sheng, Weifeng He (<i>Department of Micro-Nano Electronics, School of Electronic Information and Electronic Engineering, Shanghai Jiao Tong University</i>)
P2-27	0761: A High Performance Parallel VLSI Design of Matrix Inversion

	Kun Wang, Li Li, Feng Han, Hongbing Pan, Fan Feng, Xiao Yu (<i>School of Electronic Science and Engineering, Nanjing University</i>)
P2-29	0501: Optimization techniques to improve performance of a DDFS Look-Up table with FPGA technology Rodney Martínez Alonso, Glauco Guillen Nieto (<i>R & D, LACETEL, Boyeros</i>)
P2-30	0614: An FPGA acceleration system of exact helical CBCT image reconstruction Yan Zhang, Qi Fang, Robert K.F. Teng, Lun Gao (<i>Shenzhen Graduate School, Harbin Institute of Technology, California State University, Shenzhen University</i>)
P2-31	0674: FPGA Bitstream Compression and Decompression based on LZ77 Algorithm and BMC Technique Yuanpei Gao, Haijiang Ye, Jian Wang, Jinmei Lai (<i>State Key Laboratory of ASIC and System, Fudan University</i>)
P2-32	0736: FPGA logic design of SATA3.0 physical layer Zong Yang, Hui Xu, Nan Li, Zhaolin Sun (<i>Electronic science and engineering, National University of Defense and Technology</i>)
P2-33	0356: A High-Efficient Floating Point Coprocessor for SPARC Leon2 Embedded Processor Chen Zhao, Kuizhi Mei, Fei Wang, Nanning Zheng (<i>Institute of Artificial Intelligence and Robotics, Xi'an Jiaotong University</i>)
P2-34	0416: Performance Analysis of On-chip Bufferless Router with Multi-ejection Ports Chaochao Feng (<i>School of Computer, National University of Defense Technology, Department of Electronic Systems, Royal Institute of Technology</i>) Zhuofan Liao (<i>School of Computer and Communication Engineering, Changsha University of Science & Technology</i>) Zhonghai Lu, Axel Jantsch (<i>Department of Electronic Systems, Royal Institute of Technology</i>) Zhenyu Zhao (<i>School of Computer, National University of Defense Technology</i>)
P2-35	0422: A Deterministic Optimal Task Migration Algorithm Design in NoC-based Multi-core System Fangfa Fu, Jun Liao, Tao Li, Jinxiang Wang (<i>Microelectronics Center, Harbin Institute of Technology</i>)
P2-36	0424: A Dynamic and Low Latency Wireless NoC Architecture Yiou Chen, Xiang Ling, Jianhao Hu (<i>National Key Lab of Science and Technology on Communications, University of Electronic Science and Technology of China</i>)
P2-37	0445: A Routing Algorithm for Network-on-Chip with Self-Similar Traffic

	Wei Ni, Zhenwei Liu(<i>Institute of VLSI Design, Hefei University of Technology</i>)
P2-38	0489: A near threshold error resilient processor based on dynamic timing error prediction and Within-a-Cycle timing error correction Taotao Zhu(<i>Institute of VLSI Design, Zhejiang University</i>) Xiaoyan Xiang, Chen Chen, Jianyi Meng(<i>Department of Microelectronics, Fudan University</i>)
P2-39	0505: A Low Power and High Speed CAM Design Using Pulsed Voltage for Search-Line Song Jia, Weiting Li, Wenyi Tang, Yuan Wang(<i>Institute of Microelectronics, Peking University</i>)
P2-40	0535: An Energy-Efficient Microprocessor Using Multilevel Error Correction for Timing Error Tolerance Sheng Wang(<i>Institute of VLSI Design, Zhejiang University</i>) Xiaoyan Xiang, Chen Chen, Jianyi Meng(<i>Department of Microelectronics, Fudan University</i>)
P2-41	0581: Performance Analysis for Matrix-Multiplication Based on an Heterogeneous Multi-core SoC Yukun Song, Rui Jiao, Duoli Zhang, Dongxue Gao (<i>Institute of VLSI Design, Hefei University of Technology</i>)
P2-42	0628: Design of Low-Power FinFET-Based TCAMs with Unevenly-Segmented Matchlines for Routing Table Applications Meng-Chou Chang, Kai-Lun He (<i>Department of Electronic Engineering National Changhua University of Education</i>)
P2-43	0718: Realization of Intelligent Optimization Algorithm on IP Cores Partition for NoC Testing Yunhui Ling, Fang Liu, Ying Zhang (<i>College of Electronic and Information Engineering, Nanjing University of Aeronautics and Astronautics</i>)
P2-44	0732: Lateral Asynchronous and Vertical Synchronous 3D Network on Chip with Double Pumped Vertical Links Yuxiang Fu, Li Li, Yuang Zhang, Hongbing Pan, Feng Han, Kun Wang (<i>Institute of VLSI Design, School of Electronic Science & Engineering, Nanjing University</i>)
P2-45	0334: A SRAM-Saving Two-Stage Storage Strategy for the Coefficients Memories in HEVC encoders Leilei Huang, Wei Cheng, Xiaoyang Zeng, Yibo Fan (<i>Department of Microelectronics, Fudan University</i>)
P2-46	0350: A High-Sensitivity ASK Demodulator for Passive UHF RFID Tags with Automatic Voltage Limitation and Average Voltage Detection

	Li Yang, Lei Cai, Miao Xia Zheng (<i>School of Physics and Optoelectronics Engineering, Xiangtan University</i>), Jiancheng Li, Jian Li (<i>School of Electronic Science and Engineering, National University of Defense Technology</i>), Minghua Tang (<i>School of Material Science and Engineering, Xiangtan University</i>)
P2-47	0409: High Performance Protocol Converters for Two Phase Quasi-Delay Insensitive System-Level Communication
	Yao Peng, Xiaofei Qi (<i>School of Information Science and Technology, Northwest University</i>), Yanfei Yang (<i>School of College of Science, Xi'an Polytechnic University</i>)
P2-48	0415: Functional Coverage-Driven UVM-based UART IP Verification
	Wei Ni, Xiaotian Wang (<i>Institute of VLSI Design, Hefei University of Technology</i>)
P2-49	0417: Research of Reusability Based on UVM Verification
	Wei Ni, Jichun Zhang (<i>Institute of VLSI Design, Hefei University of Technology</i>)
P2-50	0430: A Flexible HEVC Intra Mode Decision Hardware for 8kx4k Real Time Encoder
	Yanheng Lu, Wei Cheng, Leilei Huang, Xiaoyang Zeng, Yibo Fan (<i>Department of Microelectronics, Fudan University</i>)
P2-51	0509: A Dynamic Reprogramming Scheme to Enhance the Reliability of RRAM
	Zhongyuan Xiang, Feng Zhang (<i>Institute of Microelectronics of Chinese Academy of Sciences</i>)
P2-52	0515: I/Q Imbalance Estimation in OFDM Systems
	Xuerong Zhou, Xiangyan Xue, Fan Ye, Junyan Ren (<i>State-Key Laboratory of ASIC and System, Fudan University</i>)
P2-53	0517: A New Method for Demodulation of FSK Signal with Severe Impulse Interference
	Heyi Hu, Chun Zhang, Yongming Li (<i>Department of Microelectronics and Nanoelectronics, Tsinghua University</i>)
P2-54	0519: Design and Implementation of a MAC Protocol for a Wearable Monitoring System on Human Body
	Ning Li, Ke Lin, Shanshan Yong, Xiaofei Chen, Xinan Wang (<i>The Key Lab of Integrated Microsystems Peking University Shenzhen Graduate School</i>), Xing Zhang (<i>Institute of Microelectronics, Peking University</i>)
P2-55	0531: Design and Implementation of a Body Monitoring Baseband System for Human Body Communication
	Xiaofei Chen, Bo Wang, Ke Lin, Ning Li, Chen Chen, Haibin Shao, Xin-An Wang (<i>The Key Lab of Integrated Microsystems, Peking University Shenzhen Graduate</i>)

	<i>School)</i>
P2-56	0534: An Automatic Software/Hardware Verification Platform Prototype for Reconfigurable Audio Algorithm in Media SoC Zheng Zheng, Xianan Wang, Zhaoyang Guo (<i>The Key Lab of IMS, School of ECE, Peking University Shenzhen Graduate School</i>), Guoxing Zhang (<i>Shenzhen Micro & Nano Research Institute of IC and System Applications</i>)
P2-57	0591: Network-Coding-Based Distributed Relay Scheme for PLC Networks Jiaan Dai, Xiaofang Zhou (<i>State Key Lab of ASIC & System, Fudan University</i>), Linshan Zhang (<i>YunNan Electric Power Science Test & Research Institute Group Co., Ltd</i>), Gerald E. Sobelman (<i>Department of Electrical and Computer Engineering, University of Minnesota</i>)
P2-58	0592: Design of a High Parallelism High Throughput HSPA+ Turbo Decoder Jieqiong Cheng, Qingqing Yang, Xiaofang Zhou (<i>State Key Lab of ASIC & System, Fudan University</i>)
P2-59	0617: A Lifting-based 2-D Discrete Wavelet Transform Architecture for Data Compression of Bio-potential Signals Yi Ren, Jun Han, Zhiyi Yu, Sizhong Xuan, and Xiaoyang Zeng, (<i>State Key Lab of ASIC and System, Fudan University</i>)
P2-60	0637: Generation of Low Power Testing based on Novel SIC Sequences Bei Cao (<i>Electronic Science and Technology Post-Doctoral Research Center, Heilongjiang University, Developing Key Laboratory of Sensing Technology and Systems in Cold Region of Heilongjiang Province and Ministry of Education, Heilongjiang University</i>), Zhiyuan Li, Dianzhong Wen (<i>Electronic Science and Technology Post-Doctoral Research Center, Heilongjiang University</i>)
P2-62	0698: An Improved FFT Architecture Optimized for Reconfigurable Application Specified Processor Feng Han, Li Li, Kun Wang, Fan Feng, Hongbing Pan, Dong Yu (<i>School of Electronic Science and Engineering, Nanjing University</i>)
P2-63	0716: Design of Energy Efficient LDPC Decoders with Low-Voltage Strategy Jianing Su (<i>Advanced Circuit and System Lab, Suzhou Institute of Nano-tech and Nano-Bionics, Chinese Academy of Sciences</i>), Jun Han (<i>ASIC & System State Key Lab, Department of Microelectronics, Fudan University</i>)
P2-64:	0734: An Enhanced Decoder for Multiple-Bit Error Correcting BCH Codes Hupo Wei, Xiaole Cui, Qiang Zhang, Yufeng Jin (<i>Key Lab of Integrated Microsystems, Peking University Shenzhen Graduate School</i>)

P2-65	0737: Biased MMSE Soft-Output Detection Based on Conjugate Gradient in Massive MIMO
	Jiangyun Zhou, Jianhao Hu, Jienan Chen, Shuaining He (<i>National key Lab. of Communications University of Electronic Science and Technology of China</i>)
P2-66	0747: A Viterbi Decoder for UHF RFID Digital Baseband
	He Wang, Xi Tan, Junyu Wang (<i>State Key Laboratory of ASIC & System, Fudan University</i>), Feng Chen, Chao Wang (<i>Information Center of China State Food and Drug Administration (CFDA)</i>)
P2-67	0447: A Countermeasure for Power Analysis to Scalar Multiplication of ECC Hardware
	Lifei Liu, Xiaole Cui, Yalin Ran (<i>Key Lab of Integrated Microsystems, Peking University Shenzhen Graduate School</i>), Xiaoxin Cui (<i>Institute of Microelectronics, Peking University</i>)
P2-69	0574: A ECC Crypto Engine based on Binary Edwards Elliptic Curve for Low-cost RFID Tag Chip
	Cheng Wu, Fan Yang, Xi Tan, Junyu Wang (<i>State Key Laboratory of ASIC & System, Fudan University</i>), Chao Wang, Feng Chen (<i>Information Center of China State Food and Drug Administration (CFDA)</i>)
P2-70	0632: Exploration for Energy-Efficient ECC Decoder of WBAN
	Tianchan Guan, Jun Han, Xiaoyang Zeng (<i>State Key Laboratory of ASIC & System, Fudan University</i>)
P2-71	0691: A low-cost SoC implementation of AES algorithm for bio-signals
	Zhicheng Xie, Jun Han, Jianwei Yang, Lijun Zhou, Xiaoyang Zeng (<i>State Key Laboratory of ASIC & System, Fudan University</i>)
P2-72	0695: Comprehensive Study on Higher Order Radix RSA Cryptography Engine
	Tsukasa Ikeda, Makoto Ikeda (<i>EEIS, Graduate School of Engineering, The University of Tokyo</i>)
P2-73	0735: Study and Implementation of Cluster Hierarchical Memory System of Multicore Cryptographic Processor
	Junwei Li, Zibin Dai, Wei li, Tao Chen, Yufei Zhu (<i>Department of Microelectronics, Zhengzhou Institute of Information Science and Technology</i>)

Friday

Friday, November 6, 8: 30 – 10: 00

Friday, November 6, 8: 30 – 10: 00

Wufu Hall

Keynote Session K-7 & K-8

Wufu Building1F

K-7 Wide-bandgap III-V Mixed-Signal Electronics (8: 30-9: 15)

Prof. Kevin J. Chen (Dept. of C & CE, The HongKong University of Science and Technology, HongKong)

K-8 High Design Productivity for Reliable and Energy-Efficient Circuits in the Internet of Things (9: 15-10: 00)

Prof. Deming Chen(University of Illinois, USA)

Friday, November 6, 10: 15– 12: 15

Friday, November 6, 10: 15 – 12: 15	Maesai Reception Hall Wangjiang Club 1F
Session A6 : Security Issue	
Session Chair : Han Jun, Fudan University	

	Title
A6-1	0421: Hardware Security Applications of Emerging Nonvolatile Memories (invited paper)
10: 15	An Chen (<i>GlobalFoundries</i>)
A6-2	0616: A Low Cost and High Reliability True Random Number Generator Based on Resistive Random Access Memory
10: 45	Jianguo Yang, Juan Xu, Bo Wang, Xiaoyong Xue, Yinyin Lin (<i>ASIC and System State Key Lab, Fudan University</i>), Ryan Huang, Qingtian Zhou, Jingang Wu (<i>SOC Technology Development Center, Semiconductor Manufacturing International Corp</i>)
A6-3	0478: Elliptic Curve GF(p) Point Multiplier by Dual Arithmetic Cores
11: 00	Tao Wu (<i>Wuhan Maritime Communication Research Institute</i>)
A6-4	0622: A Configurable SoC Design for Information Security
11: 15	Sizhong Xuan, Jun Han, Zhiyi Yu, Yi Ren, Xiaoyang Zeng (<i>State Key Lab of ASIC and System, Fudan University</i>)
A6-5	0639: A SIMD Multiplier-Accumulator Design for Pairing Cryptography
11: 30	Weizhen Wang, Jun Han, Jielin Wang, Xiaoyang Zeng (<i>State Key Laboratory of ASIC and System, Fudan University</i>)
A6-6	0748: High-Speed Realization of Trivium Based on Multi-Core Cryptographic Processor
11: 45	Zhouchuang Wang, Zibin Dai (<i>Department of Microelectronics, Zhengzhou Institute of Information Science and Technology</i>)
A6-7	0651: Parallel Implementation of AES on 2.5D Multicore Platform with Hardware and Software Co-Design
12: 00	Jielin Wang, Weizhen Wang, Jianwei Yang, Zhiyi Yu, Jun Han, Xiaoyang Zeng (<i>State Key Laboratory of ASIC & System, Fudan University</i>)

Friday, November 6, 10: 15 – 12: 15	Brunei Meeting Room Wangjian Club 2F
Session B6 : Wireless Communication	
Session Chair : Xiang Ling,	

University of Electronic Science and Technology of China

	Title

B6-1	0319: Linearity Enhancement Algorithms for I-Q Signal Generation (invited paper)
10: 15	Masahiro Murakami, Haruo Kobayashi, Shaiful Nizam Bin Mohyar, Takahiro Miki(<i>Division of Electronics and Informatics, Gunma</i>), Osamu Kobayashi (<i>Semiconductor Technology Academic Research Center (STARC)</i>)
B6-2	0549: A Low Complexity Algorithm and Architecture for MIMO Detection Without QR Decomposition (invited paper)
10: 45	Lian Huai, Gerald E. Sobelman (<i>Department of Electrical and Computer Engineering, University of Minnesota</i>), Samer Hijazi, Raul Casas (<i>Cadence Design Systems</i>)
B6-3	0493: A Full Layer Parallel QC-LDPC Decoder for WiMAX and Wi-Fi
11: 15	Wenchao Zhang, Song Chen, Xuefei Bai (<i>Dept. of Electronic Sci. & Tech., University of Science and Technology of China</i>), Dajiang Zhou(<i>Faculty of Science and Engineering, Waseda University</i>)
B6-4	0564: A Low Complexity MCMC Algorithm for MIMO System with Bias Technique
11: 30	Shuaining He, Jiangyun Zhou, Jianhao Hu, Jienan Chen (<i>University of Electronic Science and Technology of China</i>)
B6-5	0683: A Novel Symbol Synchronization Algorithm and Low-complexity Circuits Design for Zero-IF GFSK Demodulator
11: 45	Guanghua Wu, Hong Chen, Yanyi Meng(<i>Institute of Microelectronics, Tsinghua University</i>), Xitian Long, Kun Yang, Xueping Jiang(<i>State Grid Smart Grid Research Institute, Changping District</i>)
B6-6	0360: High-Frequency Low-Distortion Signal Generation Algorithm with Arbitrary Waveform Generator
12: 00	Shohei Shibuya, Yutaro Kobayashi, Haruo Kobayashi(<i>Division of Electronics and Informatics, Gunma University, Kiryu, Gunma</i>)

Friday, November 6, 10: 15 – 12: 15	Penang Island Meeting Room
Session C6 : SAR & $\Delta\Sigma$ ADC	Wangjiang Club 2F
Session Chair : Qiang Li, <i>University of Electronic Science and Technology of China</i>	

	Title
C6-1	0463: Automated design strategy for high performance mixed signal circuits (invited paper)
10: 15	Akira Matsuzawa(<i>Department of Physical Electronics, Tokyo Institute of Technology</i>)
C6-2	0540: A 1.8-V 12-bit Self-Calibrating SAR ADC with a Novel Comparator
10: 45	Chenxi Deng, Long Zhao, Yuhua Cheng (<i>Shanghai Research Institute of Microelectronics, Peking University, EECS Peking University</i>), Hui Zheng (<i>Shanghai</i>

	<i>Research Institute of Microelectronics, Peking University)</i>
C6-3 11: 00	0352: A 10-bit 40 MS/s Successive Approximation Register Analog-to-Digital Converter with Vcm-based Method for Wireless Communications Wen Cheng Lai (<i>Dept. of Electronic Engineering, National Taiwan Univ. of Science and Technology</i>)
C6-4 11: 15	0576: A 1-V 23-μW 88-dB DR Sigma-Delta ADC for high-accuracy and low-power applications Long Zhao, Chenxi Deng, Hongming Chen, Yuhua Cheng (<i>Shanghai Research Institute of Microelectronics, Peking University, EECS, Peking University</i>), Guan Wang (<i>Shanghai Research Institute of Microelectronics, Peking University</i>)
C6-5 11: 30	0365: Fibonacci Sequence Weighted SAR ADC Algorithm and its DAC Topology Takuya Arafune, Yutaro Kobayashi, Shohei Shibuya, Haruo Kobayashi (<i>Division of Electronics and Informatics, Gunma University</i>)
C6-6 11: 45	0643: A Lowpass/Bandpass Reconfigurable Continuous-time $\Delta\Sigma$ ADC for Software-defined Radio Xinpeng Xing (<i>Graduate School at Shenzhen, Tsinghua University</i>), Gaozhan Ca, Georges Gielen (<i>Department of Elektrotechniek, ESAT-MICAS, KU Leuven</i>)
C6-7 12: 00	0335: A 16-Bit Low-Power Double-Sampled Delta Sigma Modulator for Audio Applications Yongsheng Wang, Hongying Wan, Fengchang Lai, Yang Liu, Xiaowei Liu (<i>Micro-electronic department, Harbin Institute of Technology</i>), Bei Cao (<i>Electronic Science and technology Post-Doctoral Research Center, Heilongjiang University</i>)

Friday, November 6, 10: 15 – 12: 30	Penang MeetingRoom Wangjiang Club 2F
Session D6 : MEMS & Sensor Session Chair : Huaqiang Wu, Tsinghua University	

	Title
D6-1 10: 15	Speak Only: An Electro-chemical Sensing System for Some Biomarkers Detection from Urinary Test (invited paper) Bin-Da Liu (<i>National Cheng Kung University</i>)
D6-2 10: 45	0411: Ultra-Sensitive and Responsive Capacitive Humidity Sensor Based on Graphene Oxide Qiangqiang Ye, Chenyu Wen, Ming Xu, Shi -Li Zhang, Dongping Wu (<i>State Key Laboratory of ASIC and System, Department of Microelectronics, Fudan University,</i>)
D6-3 11: 00	0480: Humidity Sensor with Graphene Oxide as Sensing Material Xiaoxu Kang, Qingyun Zuo, Chao Yuan, Weijun Wang, Meng Gao, Liangliang

	Jiang ,Yongxing Zhou, Yong Wang, Shoumian Chen, Yuhang Zhao(<i>Process Technology Department, Shanghai IC R & D Center</i>), Jia Liu, Wenjie Sheng, Jia Zhou(<i>Department of Microelectronics, Fudan University</i>)
D6-4	0634: Droplet Generating with Accurate Volume for EWOD Digital Microfluidics
11: 15	Wei Wang, Jianfeng Chen, Jia Zhou(<i>ASIC and System State Key Lab, School of Microelectronics, Fudan University</i>)
D6-5	0608: Smartphone-controlled electro-wetting on dielectric microfluidics
11: 30	ZengZhi, Kaidi Zhang, Wei Wang, Jia Zhou (<i>State Key Laboratory of ASIC and System, Fudan University</i>), Weijiang Xu(<i>D épartement Opto-Acousto-Electronique, I.E.M.N., Universit éde Valenciennes</i>)
D6-6	0633: Application of Cellulose Triacetate as Biocompatible/ Biodegradable Dielectrics in EWOD Devices
11: 45	Lei Chao, Zhi Zeng, Kaidi Zhang, Wei Wang, Jia Zhou(<i>ASIC and System State Key Lab, School of Microelectronics, Fudan University,</i>)
D6-7	0304: System-level modeling and analysis of third order MEMS accelerometer
12: 00	Xiangliang Jin, Feng Zhang (<i>School of Physics and Optoelectronics, Xiangtan University, Hunan Engineering Laboratory for Microelectronics, Optoelectronics and System on a chip</i>)

Friday, November6, 13: 30 – 15: 30

Friday, November 6, 13: 30 – 15: 30	Maesai Reception Hall
Special Session : Devices, Systems, and Design Methodologies for IoT	
Wangjiang Club 1F	

Session Chair : Deming Chen, *University of Illinois at Urbana-Champaign*

	Title
A7-1	0801: Challenges and Future Trends for Embedded Security in Electric Vehicular Communication (invited paper)
13: 30	Yi Wang, Zhiqian Hong, Jun Li, Shaobo Luo, Yajun Ha (<i>Institute for Infocomm Research (I2R), Singapore</i>)
A7-2	0802: Challenges in design wearable wireless sensors in healthcare IoT (invited paper)
13: 45	Yong Lian (<i>Department of Electrical and Computer Engineering, York University, Toronto, Canada</i>)
A7-3	0803: System-Level Design Solutions Enabling the IoT Explosion (invited paper)
14: 00	Liwei Yang (<i>School of Computer Engineering, Nanyang Technological University</i>),

	<p>Yao Chen (<i>College of Electronic Information and Optical Engineering, Nankai University</i>), Wei Zuo (<i>University of Illinois at Urbana-Champaign</i>), Tan Nguyen,, Swathi Gurumani, Kyle Rupnow(<i>Advanced Digital Sciences Center, Singapore</i>), Deming Chen (<i>University of Illinois at Urbana-Champaign</i>)</p>
A7-4	0804: Quantitative Performance and Power Analysis of LTE using High Level Synthesis (invited paper)
14: 15	Yun Liang, Shuo Wang (<i>School of EECS, Peking University, China</i>)

Friday, November 6, 13: 30 – 15: 30	Brunei Meeting Room Wangjiang Club 2F
Session B7 : Design Verification and DFT Session Chair : Letian Huang, <i>University of Electronic Science and Technology of China</i>	

	Title
B7-1	0567: Multi-Technology Simulation with Mixed Design Environments (invited paper)
13: 30	Bin Wan, Cindy Zhang, Xingang Wang(<i>Skyworks Solutions, Inc., Irvine, California, United States</i>)
B7-2	0528: A Fast Vector Reuse Verification Method for Standard Cell Library
14: 00	Ligang Hou, Jingsong Zhi, Lin Zhu, Jinhui Wang, Xiaohong Peng, Shuqin Geng(<i>VLSI & System Lab, Beijing University of Technology</i>)
B7-3	0588: Image Synthesis Circuit Design Using Selector-logic-based Alpha Blending and Its FPGA Implementation
14: 15	Keita Igarashi, Masao Yanagisawa, Nozomu Togawa(<i>Dept. of Computer Science and Communications Engineering, Waseda University</i>)
B7-4	0770: An Automated Test Framework for SRAM-based FPGA
14: 30	Lv Xuemin(<i>School of Economics and Management, Ningbo University of Technology</i>), Yang Moucheng, Zhou Xuegong, Wang Lingli(<i>State Key Lab of ASIC and System, Fudan University</i>)
B7-5	0441: An Efficient Layered ABV Methodology for Vision System on Chip based on Heterogeneous parallel Processors
14: 45	Victor Nshunguyimfura, Jie Yang, Liyuan Liu, Nanjian Wu(<i>State Key Laboratory for Superlattices and Microstructures, Institute of Semiconductors, Chinese Academy of Sciences</i>)
B7-6	0777: Speed Up an x86 SAME Simulator Using Synthesizable SystemC Timing Model
15: 00	Jianfeng An(<i>School of Computer Science and Technology Northwestern Polytechnical University</i>), Wenxiang Li(<i>School of Computer Science and Technology Northwestern</i>)

	<i>Polytechnical University), Yi Wang(Institute for Infocomm research (I2R) A*STAR, Singapore)</i>
B7-7	0432: A High-efficient and Accurate Fault Model Aiming at FPGA-based AES Cryptographic Applications
15: 15	Nan Liao, Xiaoxin Cui, Tian Wang, Kai Liao, Yewen Ni, Dunshan Yu (<i>Institute of Microelectronics, Peking University</i>), Xiaole Cui (<i>Key Lab of Integrated Microsystems, Peking University Shenzhen Graduate School</i>)

Friday, November 6, 13: 30 – 15: 30	Penang Island Meeting Room
Session C7 : Clock module & TDC	Wangjiang Club 2F
Session Chair : Akira Matsuzawa, Tokyo Institute of Technology	

	Title
C7-1	0798: Cell-Based Programmable Phase Shifter Design For Pulsed Radar SoC (invited paper)
13: 30	Jinn-Yann, Liu Shi-Yu Huang, Ta-Shun Chu(<i>EE Dept., National Tsing Hua University, Taiwan</i>)
C7-2	0364: Reliability Concerns on Time-to-Digital Converter Due to Bias Temperature Instability in Nanometer Era
14: 00	Xinsheng Wang(<i>School of Astronautics, Harbin Institute of Technology, School of Information and Electrical Engineering, Harbin Institute of Technology</i>), Lifeng Shang, Heyi Yin(<i>School of Astronautics, Harbin Institute of Technology</i>)
C7-3	0403: A Novel Direct Digital Frequency Synthesizer Employing Complementary Dual-Phase Latch-Based Architecture
14: 15	Abdel Martinez Alonso, Masaya Miyahara , Akira Matsuzawa(<i>Department of Physical Electronics, Tokyo Institute of Technology.</i>)
C7-4	0429: An 8-bit 4fs-step Digitally Controlled Delay Element with Two Cascaded Delay Units
14: 30	Weizhen Wang, Hao Zhou, Fan Ye, Junyan Ren(<i>State Key Laboratory of ASIC and Systems, Fudan University</i>)
C7-5	0612: A Low Power TDC with 0.5ps Resolution for ADPLL in 40nm CMOS
14: 45	Xusong Liu, Lei Ma, Junhui Xiang, NaYan(<i>State Key Lab. Of ASIC and System, Dept. of Microelectronics, Fudan University</i>), Haolv Xie, Xiaowei Cai(<i>Zhongxing Telecommunication Equipment Corporation</i>)
C7-6	0635: A Digitally Calibrated Low-power Ring Oscillator
15: 00	Ming Li, Haibin Yin, Peiyuan Wan(<i>Beijing Embedded System Key Lab, Beijing University of Technology</i>)

C7-7	0511: A 400mV Supply Voltage Self-Start Clock Generator for Energy Harvest System
15: 15	Yanqin Chen, Hongguang Zhang, Xu Guo, Zhiliang Hong(<i>ASIC Laboratory 1, Fudan University</i>)

Friday, November 6, 13: 30 – 15: 30	Penang Meeting Room Wangjiang Club 2F
Session D7 : Memory 2	
Session Chair : Jiang Yan, <i>Institute of Microelectronics of Chinese Academy of Sciences</i>	

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D7-1	0783: Recent Progresses of STT Memory Design and Applications (invited paper)
13: 30	Bonan Yan, Yaojun Zhang, Enes Eken, Yiran Chen (<i>Department of Electrical and Computer Engineering, University of Pittsburgh</i>), Wujie Wen (<i>Department of Electrical and Computer Engineering, Florida International University</i>), Weisheng Zhao (<i>Spintronics Interdisciplinary Center, Beihang University</i>)
D7-2	0558: An Experimental Study on the Potential Use of ReRAM as SSD Buffer
14: 00	Mengnan Wu, Yang Yang, Xinxin Zhang, Hongbin Sun, Ruizhi Zhang, Nanning Zheng (<i>School of Electronic and Information Engineering Xi 'an Jiaotong University</i>), Liangliang Dai, Jianxiao Wang (<i>School of Electrical Engineering Xi 'an Jiaotong University</i>)
D7-3	0600: A Design of Subthreshold SRAM Cell Based on RSCE and RNCE
14: 15	Jiangzheng Cai, Jia Yuan, Liming Chen, Yong Hei (<i>ASIC & System Department, Institute of Microelectronics of Chinese Academy of Sciences</i>)
D7-4	0697: A High Efficiency All -PMOS Charge Pump for 3D NAND Flash Memory
14: 30	Liyin Fu, Yu Wang, Qi Wang, Shiyang Yang, Yan Yang, Zongliang Huo (<i>Institute of Microelectronics, Chinese Academy of Sciences</i>)
D7-5	Resistive Random Access Memory with High Selectivity ratio (invited paper)
14: 45	Sung Hyun Jo, Hagop Nazarian (<i>VP Engineering & Co-Founder, Crossbar, Inc., USA</i>)

Friday, November 6, 15: 45 – 17: 45	
Friday, November 6, 15: 45 – 17: 45	Maesai Reception Hall
Special Session : Circuits and Systems for 5G	Wangjiang Club 1F
Session Chair : Chuan Zhang, Southeast University	

	Title
A8-1	0605: OFDM Synchronization implementation based on Chisel platform for 5G

	research (Invited paper)
15: 45	Ziqiang Li, Yun Chen, Xiaoyang Zeng(<i>Department of Microelectronics, Fudan University</i>)
A8-2	0619: A high performance massive MIMO detector based on Log-domain Belief-Propagation (Invited paper)
16: 05	Kaining Han, Jianhao Hu, Jienan Chen, Sheng Yang (<i>National key Lab. Of Communications, University of Electronic Science and Technology of China</i>)
A8-3	0781: A Programmable Baseband Processor for Massive MIMO Uplink Multi-User Detection (Invited paper)
16: 25	Xiaoying Qiu, Leilei Miao, Runbin Shi, Zhiwei Wang, Di Wu (<i>School of Electronics and Information Engineering, Soochow University</i>), Liang Liu(<i>Lund University</i>)
A8-4	0794: Efficient Early Termination Schemes for Belief-Propagation Decoding of Polar Codes (Invited paper)
16: 45	Yuanrui Ren(<i>National Mobile Communications Research Laboratory, Southeast University, School of Electronic Science and Engineering, Nanjing University</i>), Chuan Zhang, Xiaohu You (<i>National Mobile Communications Research Laboratory, Southeast University</i> ,), Xing Liu(<i>Huawei Technologies Cooperation Limited, Shenzhen</i>)
A8-5	0795: Circuits and Systems for 5G Network: Massive MIMO and Advanced Coding (Invited paper)
17: 05	Liang Liu (<i>Department of Electrical and Information Technology, Lund University</i>), Chuan Zhang(<i>National Mobile Communications Research Laboratory, Southeast University</i>)
A8-6	0796: Coefficient Adjustment Matrix Inversion Approach and Architecture for Massive MIMO Systems (Invited paper)
17: 25	Xiao Liang, Chuan Zhang, Xiaohu You (<i>National Mobile Communications Research Laboratory, Southeast University</i>), Shugong Xu(<i>Intel Collaborative Research Institutes on Mobile Networking and Computing, Intel Labs</i>)

Friday, November 6, 15: 45 – 17: 45	Brunei Meeting Room
Session B8 : Other Design Topics	Wangjiang Club 2F
Session Chair : Yun Liang, Peking University	

	Title
B8-1	0425: Employing the mixed FBB/RBB in the design of FinFET logic gates
15: 45	Tian Wang, Xiaoxin Cui, Kai Liao, Nan Liao, Yewen Ni, Dunshan Yu (<i>Institute of Microelectronics, Peking University</i>), Xiaole Cui(<i>Key Lab of Integrated Microsystems, Peking University Shenzhen Graduate School</i>)

B8-2	0678: Low-Cost Low-Power Droop-Voltage-Aware Delay-Fault-Prevention Designs for DVS Caches
16: 00	Pei-Yuan Chou,I-Chen Wu,Jai-Wei Lin,Xuan-Yu Lin,Jinn-Shyan Wang (<i>SoC/AIMHI Research Centers and Dept. of EE, Nat 'l Chung-Cheng University, Chia-Yi), Tien-Fu Chen (Dept. CS, Nat 'l Chiao-Tung University, Hsin-Chu), Tay-Jyi Lin (SoC/AIMHI Research Centers and Dept. of CS, Nat 'l Chung-Cheng University, Chia-Yi)</i>)
B8-3	0532: DCPG: Double-Control Power Gating Technique for a 28 nm Cortex™-A9 MPCore Quad-core Processor
16: 15	Qian Liang, Peiyuan Wan, Ligang Hou (<i>VLSI and System Lab, Beijing University of Technology, Beijing</i>), Jinhui Wang (<i>VLSI and System Lab, Beijing University of Technology, Beijing, Department of Electrical and Computer Engineering, North Dakota State University</i>), Na Gong (<i>Department of Electrical and Computer Engineering, North Dakota State University</i>)
B8-4	0582: A 4th-Order N-path Filter in 40nm CMOS with Tunable Gm-C Stage
16: 30	Rundao Lu, Zhijian Lu, Dongpo Chen, Tingting Mo (<i>Center for Analog/RF Integrated Circuits (CARFIC), School of Microelectronics Shanghai Jiao Tong University</i>)
B8-5	0717: A Low Power 1.5GHz Gm-C Filter with 40dB Variable Gain in 65-nm CMOS Technology
16: 45	Haoyu Mei, Wei Li (<i>State Key Laboratory of ASIC & System, Fudan University</i>)
B8-6	0583: A Dual-Band Frequency Tunable Complex Filter with Stable Quality-Factor in Different Temperatures
17: 00	Suoping Hu, Dongpo Chen, Tingting Mo (<i>Center for Analog/RF Integrated Circuits (CARFIC), School of Microelectronics Shanghai Jiao Tong University</i>)
B8-7	0419: Selectable Notch Frequency of EMI Spread Spectrum using Pulse Modulation in Switching Converter
17: 15	Yasunori Kobori (Dep. Of Innovative Electrical and Electronic Engineering, National Institute of Technology, Oyama College, Oyama, Tochigi, Japan, Division of Electronicsand Informatics, Gunma University, Kiryu, Gunma,Japan) Takuya Arafune, Nobukazu Tsukiji, Nobukazu Takai, Haruo Kobayashi (Division of Electronicsand Informatics, Gunma University, Kiryu, Gunma,Japan)
B8-8	0485: EMI Reduction by Analog Noise Spread Spectrum In Ripple Controlled Switching Converter
17: 30	Yasunori Kobori, Taifeng Wang, Nobukazu Tsukiji, Nobukazu Takai, Haruo Kobayashi (<i>Division of Electronics and Informatics, Gunma University, Gunma,Japan</i>)

Friday, November 6, 15: 45 – 17: 45

Penang Island Meeting Room

Session C8: PLL

Wangjiang Club 2F

Session Chair : Shaowei Zhen,

University of Electronic Science and Technology of China

	Title
C8-1	0341: A PVT Variation Tolerant and Low Power 5Gb/s Clock and Data Recovery Circuit For PCI-E 2.0/USB 3.0
15: 45	Feng Zhang, Hao Ju, Chengying Chen (<i>Institute of Microelectronics, Chinese Academy of Science</i>)
C8-2	0325: Implementation of Digital Delta Sigma Modulator and a Divider Circuit for Fractional-N PLL
16: 00	Manas Kumar Hati, Tarun K. Bhattacharyya (<i>Advanced Technology Development Centre, IIT Kharagpur, India</i>)
C8-3	0442: A High-Performance Charge Pump with Improved Static and Dynamic Matching Characteristic
16: 15	Haibin Shao, Ke Lin, Bo Wang, Chen Chen, Fang Gao, Feng Huang, Xinan Wang (<i>The Key Laboratory of Integrated Microsystems, Peking University Shenzhen Graduate School</i>)
C8-4	0455: A Wideband VCO with Constant Tuning-Gain and Uniform Sub-Band Interval for Single-Chip UHF RFID Reader
16: 30	Jianqiao Tang, Runxi Zhang, Chunqi Shi (<i>Institute of Microelectronic Circuits & Systems, East China Normal University</i>)
C8-5	0585: A GHz-Level Ring-Counter-Based Multi-Modulus Fractional LO Divider with On-the-Fly Tunability
16: 45	Bukun Pan, Jing Jin, Jianjun Zhou (<i>Center for Analog/RF Integrated Circuits (CARFIC), School of Microelectronics, Shanghai Jiao Tong University</i>)
C8-6	0673: A 6-13 GHz Wide-tuning-range Low-phase-noise Ring Oscillator Utilizing Frequency Multiplication Technique
17: 00	Bowen Yang, Zhijian Lu, Jianjun Zhou (<i>Center for Analog/RF Integrated Circuits (CARFIC), School of Microelectronics, Shanghai Jiao Tong University</i>)
C8-7	0766: Improvement of the charge pump for Maneatis PLLs
17: 15	Zhan Shi, Zhenan Tang, Fan Yang, Jiarui Wu (<i>School of Electronic Science and Technology, Dalian University of Technology</i>)

Friday, November 6, 15: 45 – 17: 45

Penang Meeting Room

Session D8 : Advanced Process and Devices

Wangjiang Club 2F

Session Chair : Guangxi Hu, *Fudan University*

	Title
D8-1	0439: Advanced Germanium Channel Transistors (invited paper)
15: 45	C.W. Liu (<i>Graduate Institute of Electronic Engineering, National Taiwan University, National Nano Device Laboratories</i>), I.-H. Wong, S.-H. Huang, C.-H. Huang (<i>Graduate Institute of Electronic Engineering, National Taiwan University</i>), S.-H. Hsu (<i>National Nano Device Laboratories</i>)
D8-2	0631: A Simulation Analysis of Back Gate Effects for FDSOI Devices
16: 15	Yudong Li, Bo Tang, Jiang Yan (<i>Institute of Microelectronics of Chinese Academy of Sciences</i>)
D8-3	0466: A TSV Alignment Design for Multilayer 3D IC
16: 27	Wei Zhao, Ligang Hou, Xiaohong Peng, Jinhui Wang, Jingyan Fu, Yang Yang (<i>VLSI & System Lab, Beijing University of Technology</i>)
D8-4	0542: 3D Resist Modeling for OPC Correction and Verification
16: 39	Liang Zhu, Neo Tan, Zhibo Ai (<i>Synopsys Inc., Shanghai</i>), Qian Ren (<i>Synopsys Inc., Hillsboro, Oregon, USA</i>)
D8-5	0550: A Thermal-Aware Distribution Method of TSV in 3D IC
16: 51	Ligang Hou, Jingyan Fu, Wei Zhao, Shuqin Geng (<i>VLSI and System Lab, Beijing University of Technology</i>), Jinhui Wang (<i>VLSI and System Lab, Beijing University of Technology, Department of Electrical and Computer Engineering, North Dakota State University</i>), Na Gong (<i>Department of Electrical and Computer Engineering, North Dakota State University</i>)
D8-6	0381: Investigation of a GaN-on-Si HEMT optimized for the 5th-generation wireless communication
17: 03	Hong-Fan Huang, Xiao-Yong Liu, Jin-Shan Shi, Lin-Qing Zhang, Sheng-Xun Zhao, Min-Zhi Lin, Peng-Fei Wang (<i>State Key Laboratory of ASIC and System, Fudan University</i>), Bin Wu (<i>Jiangsu Changjiang Electronics Technology Co.,Ltd</i>)
D8-7	0681: Effect of Field Implantation on Off- and On-State Characteristics for Thin Layer SOI Field P-Channel LDMOS
17: 15	Xin Zhou, Yang Li, Zhaoji Li, Bo Zhang (<i>State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China</i>), Ming Qiao (<i>State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, The Institute of Electronic and Information Engineering in Dongguan, University of Electronic Science and Technology of China</i>)
D8-8	0380: TCAD simulations of Novel Interrupted-P-Finger UV/Blue Photodiode based on CMOS PROCESS
17: 27	Xiangliang Jin, Zhenyu Jiang, Manfang Tian (<i>Faculty of Materials, Optoelectronics</i>)

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ASICON 2015 Technical Program Overview

Date	Time	Maesai Reception Hall Wangjiang Club, 1F	Brunei Meeting Room Wangjiang Club, 2F	Penang Island Meeting Room Wangjiang Club, 2F	Penang Meeting Room Wangjiang Club, 2F
Nov. 3	8: 30-10: 00	Tutorial Session T-1	Tutorial Session T-4		
	10: 15-12: 15	Tutorial Session T-2	Tutorial Session T-5		
	13: 30-16: 30	Tutorial Session T-3	Tutorial Session T-6		
Nov. 4	8: 30-9: 00			Opening	
	9: 00-10: 30			Keynote Session K-1 & K-2 (Wufu Hall, Wufu Building, 1 F)	
	10: 45-12: 15			Keynote Session K-3 & K-4 (Wufu Hall, Wufu Building, 1 F)	
	13: 30-15: 30	Session A1 Image & Sound Processing	Session B1 Digital Module	Session C1 RF Circuit 1	Session D1 Power Management
	15: 45-17: 45	Session A2 Special Session : Advanced ESD Protection Design for ICs	Session B2 System-Level Design Methodology	Session C2 Other ADC & DAC Module	Session D2 Wireless Communication
	17: 45-18: 45			Poster Session 1 (Wufu Building, 1F)	
	19: 00-21: 00			Reception (Songtao Room, Wufu Building, 1F)	
Nov. 5	8: 30-10: 00			Keynote Session K-5 & K-6 (Wufu Hall,Wufu Building , 1F)	
	10: 15-12: 15	Session A3 Implantable Device & IoT	Session B3 Signal Processing & Filter	Session C3 Flash & Pipelined ADC	Session D3 Reliability & Device Topics
	13: 30-15: 30	Session A4 Micro Processor & NOC	Session B4 Circuit Optimization and Physical Design Automation	Session C4 RF Circuit 2	Session D4 Memory1
	15: 45-17: 45	Session A5 Special Session : THz Communication and Sensing	Session B5 Chip Test & Reliability	Session C5 Analog Circuit	Session D5 High Power Device
	17: 45-18: 45			Poster Session 2 (Wufu Building ,1F)	
Nov. 6	8: 30-10: 00			Keynote Speech K-7 & K-8 (Wufu Hall ,Wufu Building , 1F)	
	10: 15-12: 15	Session A6 Security Issue	Session B6 Wireless Communication	Session C6 SAR & $\Delta\Sigma$ ADC	Session D6 MEMS & Sensor
	13: 30-15: 30	Session A7 Special Session : Devices, Systems, and Design Methodologies for IoT	Session B7 Design Verification and DFT	Session C7 Clock module & TDC	Session D7 Memory2
	15: 45-17: 45	Session A8 Special Session : Circuits and Systems for 5G	Session B8 Other Design Topics	Session C8 PLL	Session D8 Advanced Process and Devices
	19: 00-21: 00			Banquet (Songtao Room, Wufu Building, 1F)	